Assessing General-Purpose Processors for DSP Applications

Part I: Architectural Approaches

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Why Are GPPs Adding DSP?

- An increasing number of applications include a mixture of microcontroller/DSP tasks, which (until recently) meant using two processors. For example:
  - Cell phones use a DSP for voice processing and a μC for supervisory control
  - PCs use dedicated DSPs for audio & telecom processing, plus a host processor for general computing
- Using one processor for both tasks can potentially reduce cost, power consumption, and system complexity

Considerations for the DSP Wannabe

- DSP performance
- Execution-time predictability
  - Difficulties ensuring real-time performance
  - Difficulties optimizing software
- Cost
- Memory bandwidth
- Power consumption
- Development tools, DSP software libraries

A Spectrum of DSP Enhancements

No change
- PowerPC 604e

Minor changes to ISA
- R4650
- ColdFire

Architectural renovation
- SH-DSP
- MMX
- AltiVec

Co-processor
- Piccolo

Totally new design
- TriCore
- Hyperstone

BDTi

No Change: PowerPC 604e

- High-performance GPP with no DSP modifications
  - 4-way superscalar execution
  - Branch prediction
  - Floating-point datapath
  - Very high clock rate (333 MHz)
- All this adds up to extremely good DSP performance, in spite of a lack of DSP enhancements

PowerPC 604e

Advantages

- Already present in a number of systems (Macs, etc)
- Very strong DSP performance

Disadvantages

- Dynamic features kill execution-time predictability, complicate software optimization
- No DSP-specific development tools
- Expensive

Minor ISA Tweaks: R4650

- Low-cost GPP for embedded applications
- Single-issue 64-bit RISC CPU
- ISA enhanced by MAC instruction & cache-locking feature
- No substantive DSP-oriented hardware enhancements
  - Memory bandwidth not increased to support MAC instruction
- Good DSP performance by virtue of high clock speeds & powerful MCU architectecture, not because of DSP enhancements

R4650

Advantages

- Predictable execution times
- Simple instruction set
- Simple programming model
- Performance comparable to dedicated DSPs
- C compilers, software readily available--substantial infrastructure already in place

Disadvantages

- Lack of increase in memory bandwidth renders MAC instruction somewhat impotent

DSP Renovation: SH-DSP

- Microcontroller (SH-2) augmented for DSP
- A major renovation in both hardware and software
  - Added a fixed-point DSP datapath
  - Harvard architecture
  - Added DSP-oriented addressing modes, dedicated address-generation hardware
  - Second set of registers for DSP unit
  - Fairly complete DSP instruction set
  - One instruction stream; DSP and MCU data paths cannot operate in parallel

SH-DSP

Advantages

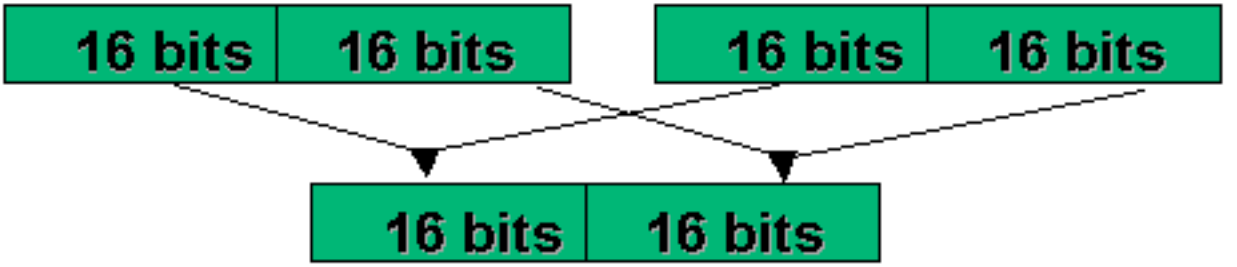
- Includes most features found in conventional DSP processors, plus a microcontroller
- Ability to run existing μC code without modifications
- Predictable execution times
- DSP development tools available
- Strong DSP performance (i.e., comparable to many dedicated DSPs)

Disadvantages

- More complicated programming model than dedicated DSPs
- Can't execute μC & DSP tasks simultaneously
- Higher cost than comparable dedicated DSPs

SIMD Renovation: MMX, AltiVec

- What's SIMD?



- High-performance GPPs often have
  - Superscalar execution
  - Branch prediction
  - Floating-point data path
  - Very high clock rates (266+ MHz)

MMX, AltiVec

Advantages

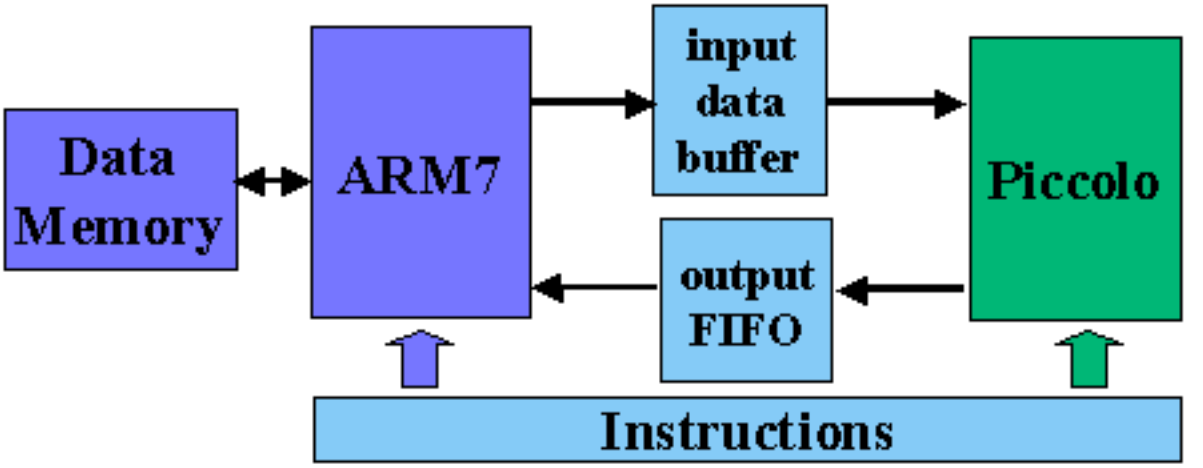
- Very strong DSP performance; better than most DSPs
- Already present in a number of systems (PCs, etc)
- Strong development tool support

Disadvantages

- Lack of execution-time predictability
- Few DSP-oriented tools
- Expensive
- SIMD only good for certain types of processing
- Power-hungry

DSP Coprocessor: ARM Piccolo

- Separate DSP co-processor core meant to be used with an ARM7 μC
  - Fixed-point DSP datapath with standard DSP features
  - Separate DSP-oriented instruction set
  - Separate instruction stream
  - Relies on ARM7 to transfer data to/from memory via buffers



ARM Piccolo

Advantages

- Can add DSP capabilities to existing ARM7 designs without code modification
- Dedicated DSP hardware provides good DSP performance, comparable to midrange DSPs
- ARM7 & Piccolo can operate in parallel in some cases

Disadvantages

- Piccolo performance is limited by ARM7's memory bandwidth (von Neumann memory architecture)
- Complicated programming model: two instruction streams, two instruction sets, possible deadlocks

New Architecture: TriCore

- Designed as a hybrid MCU/DSP from the ground up
- Superscalar RISC microprocessor
- SIMD operations
- Unified instruction set for both control code and DSP code
- Targets 100 MHz; not yet in silicon

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Part II: Benchmark Comparisons

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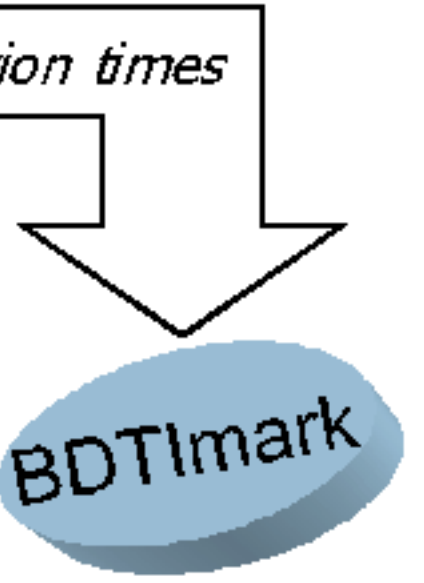
BDTI Benchmarking Methodology

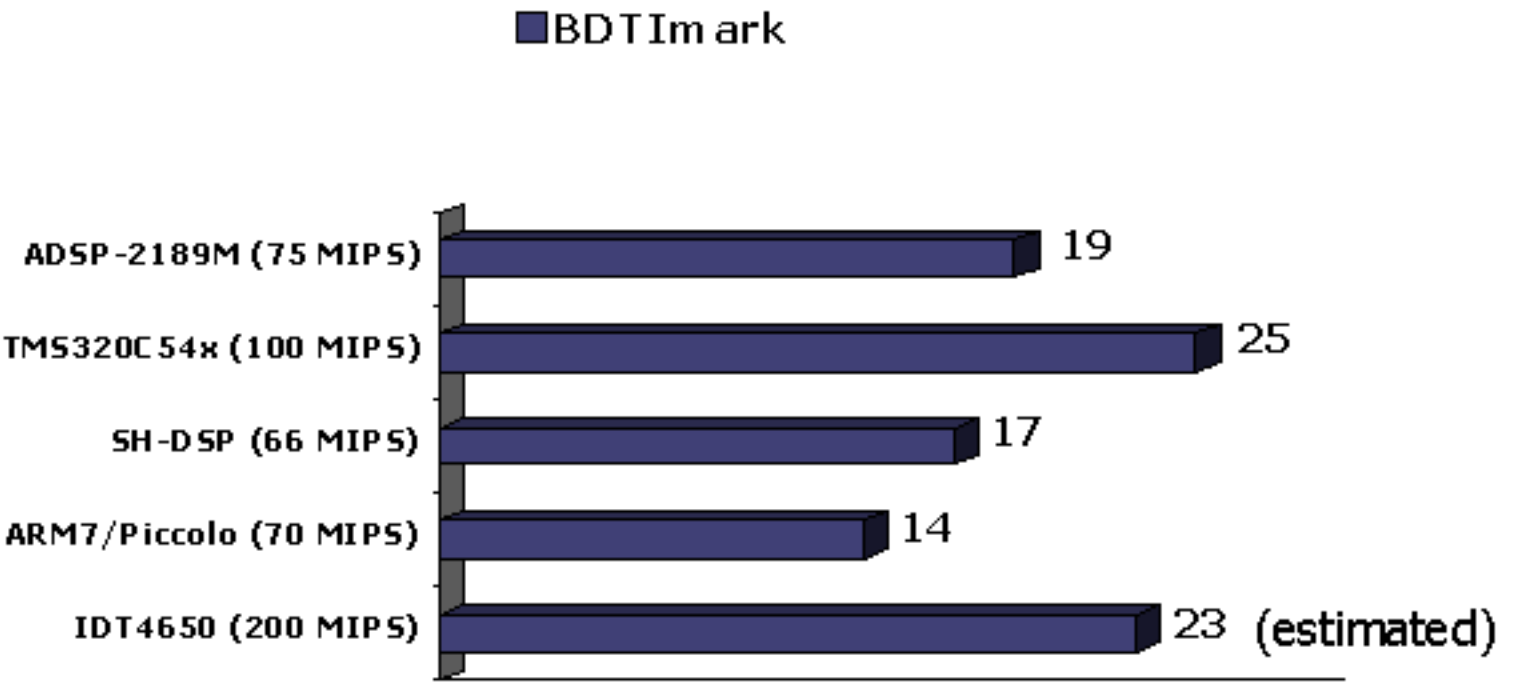
- BDTI's benchmarks consist of 11 DSP algorithm "kernels"
- Benchmarks are rigorously defined; all implementations follow the same rules
- Benchmarks are hand-optimized in assembly code
- Benchmarks optimized for speed, then memory use
- Benchmarks reveal realistic performance, not necessarily fastest possible performance
- Benchmarks are architecture-independent; can be implemented on any processor (even non-DSPs)

The BDTImark

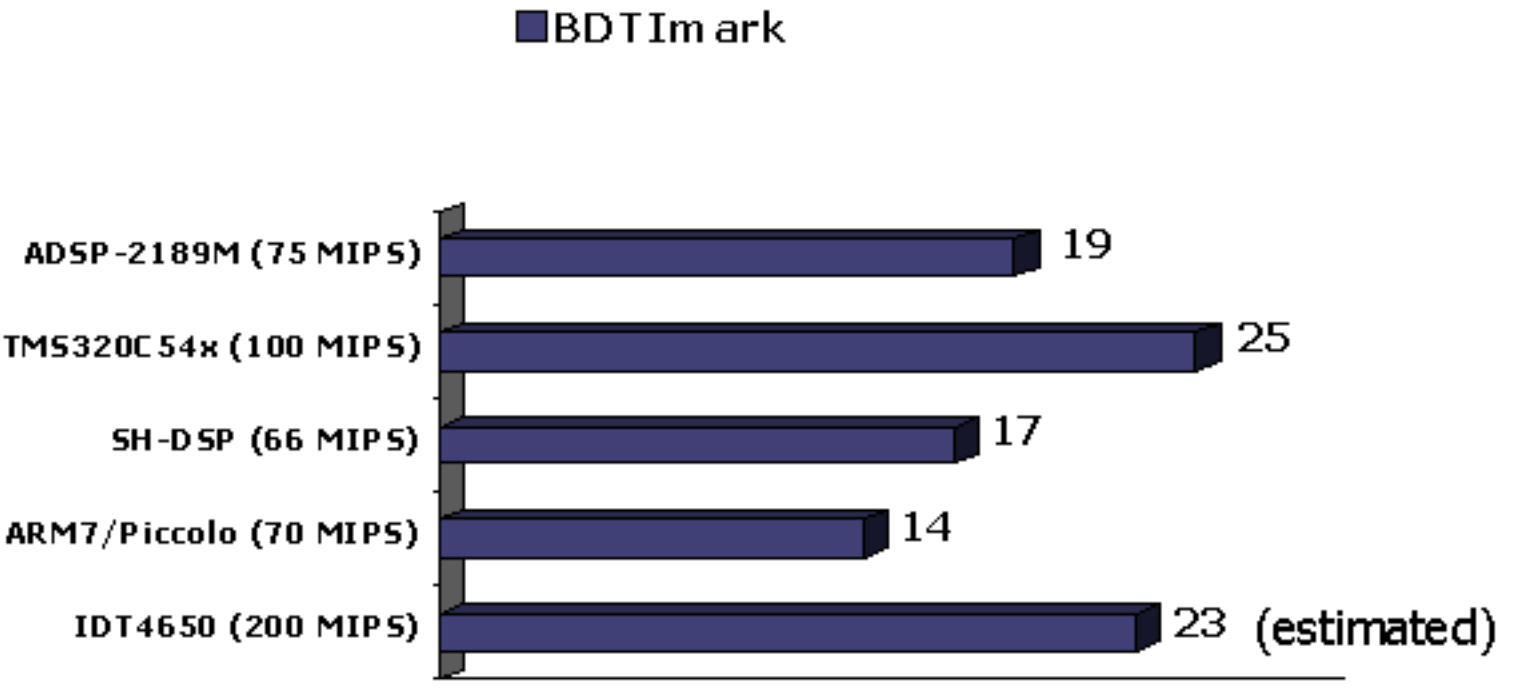
Real block FIR filter
Complex block FIR filter
Single-sample real FIR filter
Single-sample LMS-adaptive FIR filter
Single-sample IIR filter
Vector dot product
Vector add
Vector maximum
IS-54 convolutional encoder
Finite state machine
256-point FFT



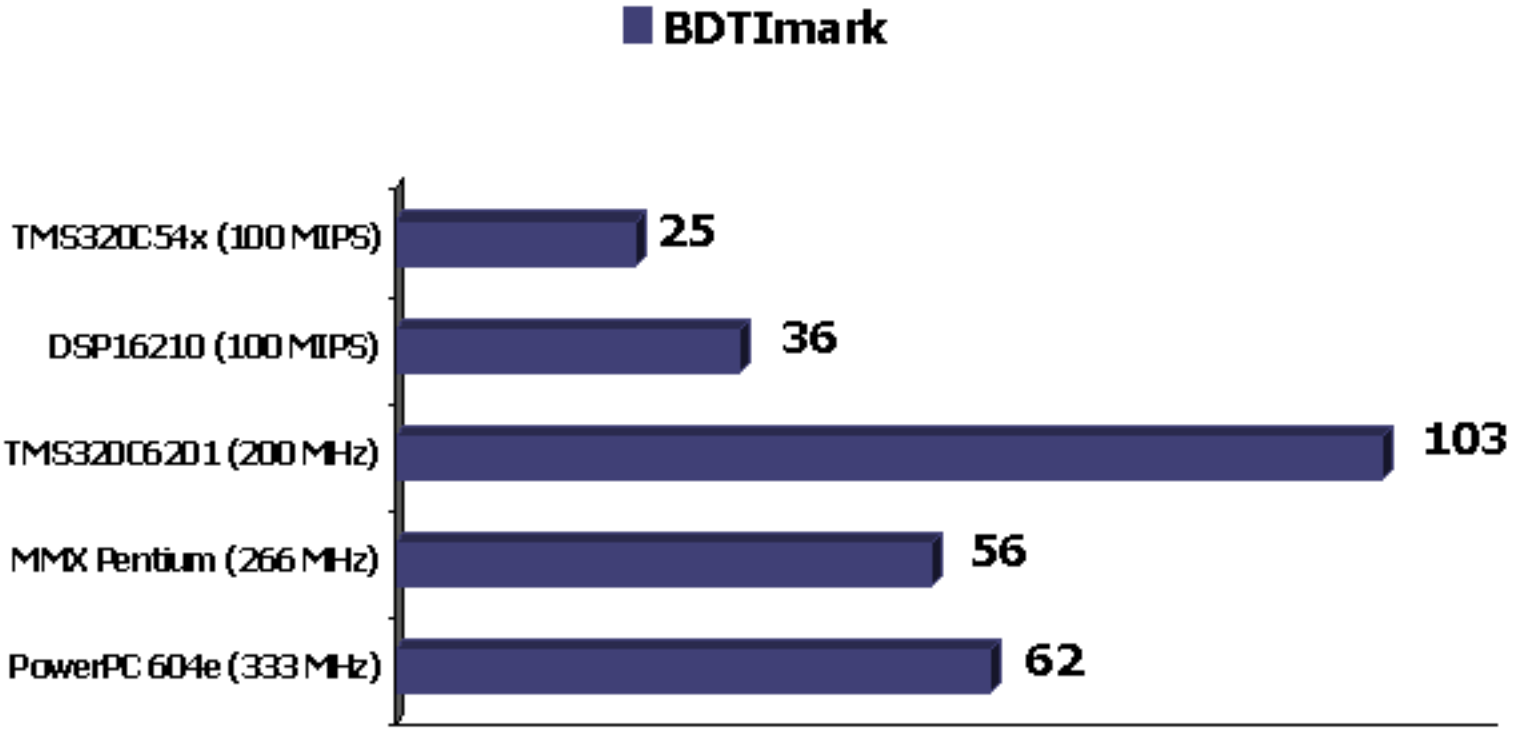
Benchmark Results: Speed



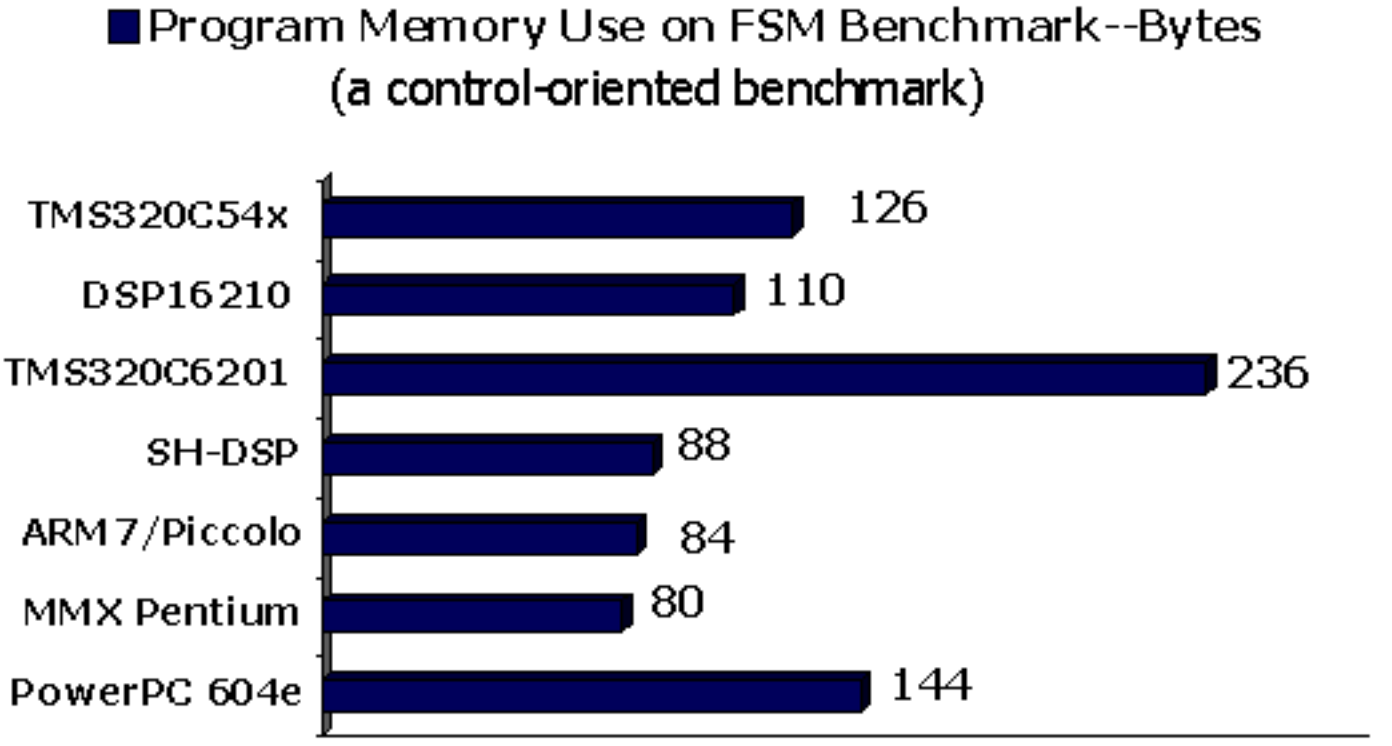
Benchmark Results: Speed



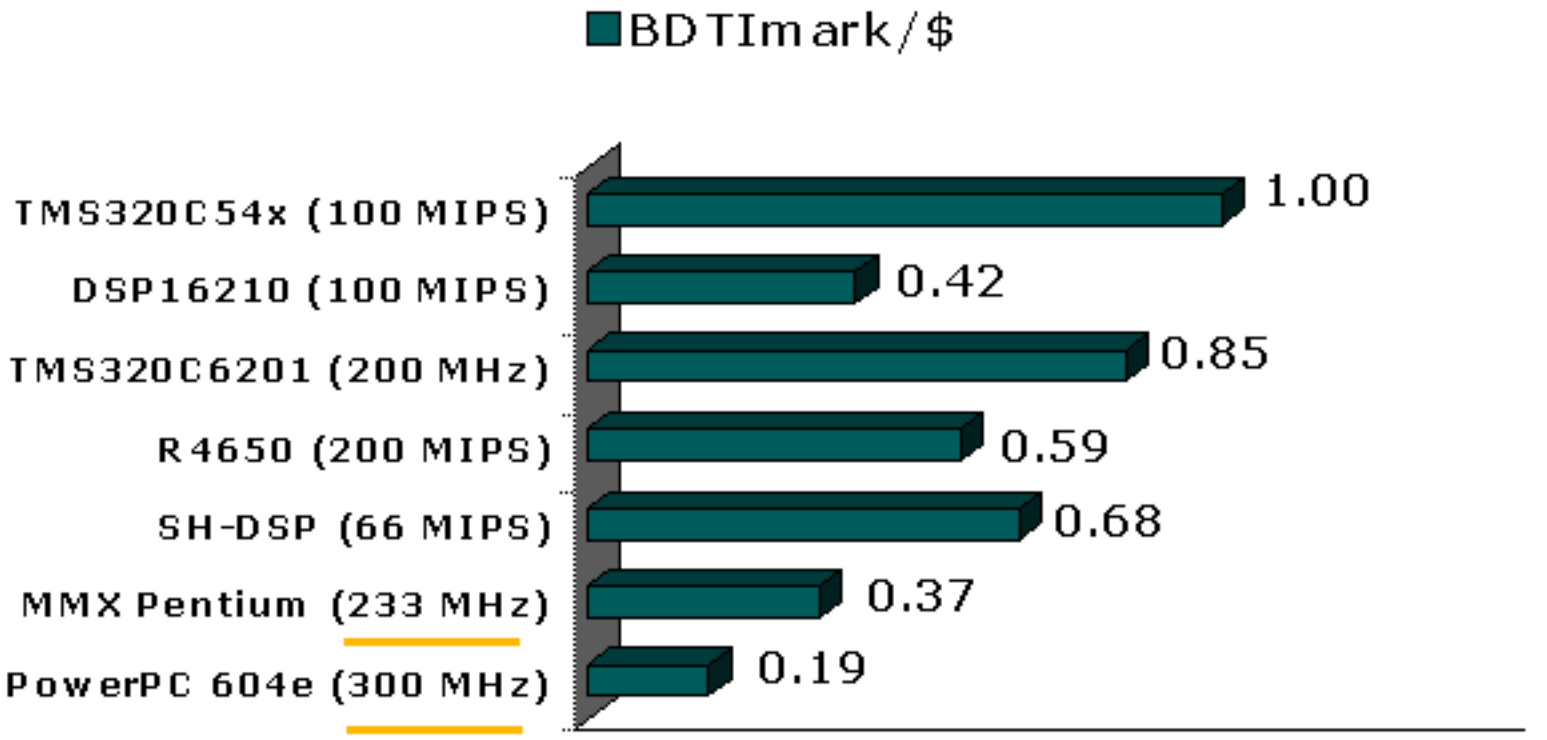
Benchmark Results: Speed



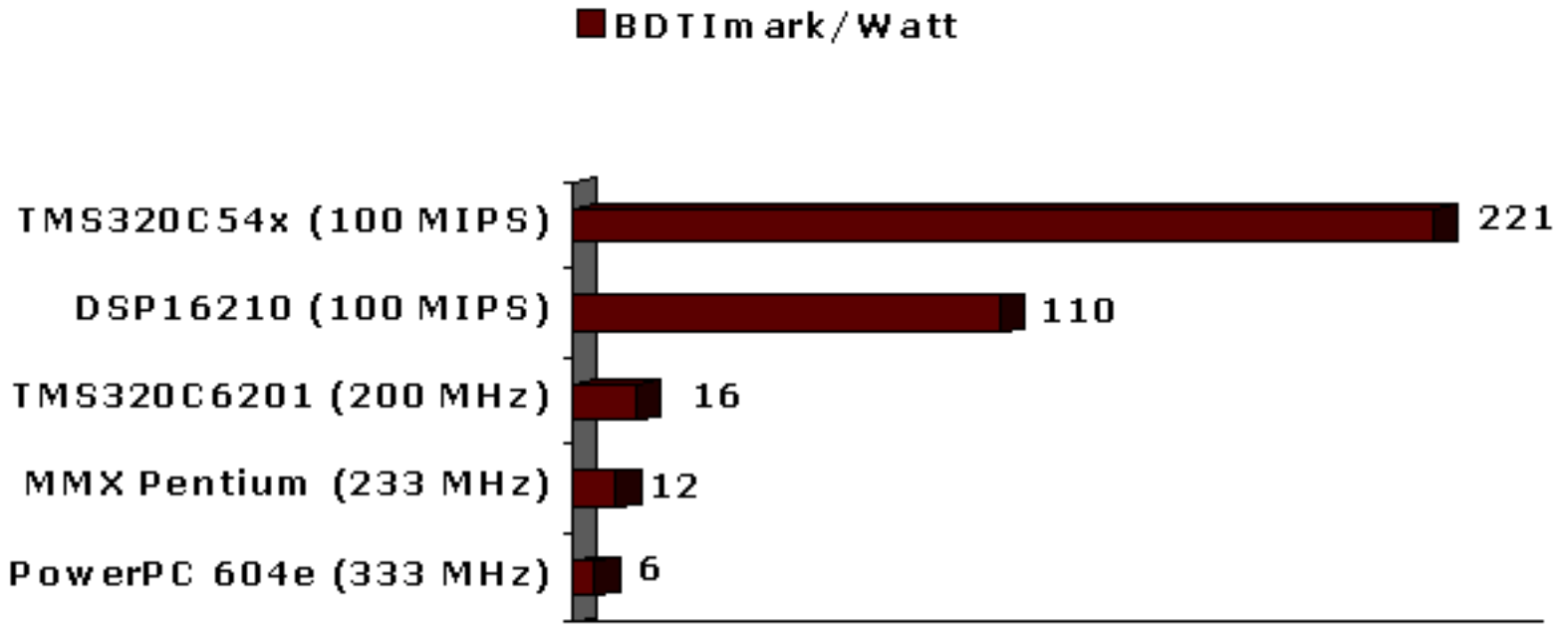
Benchmark Results: Memory Use



Benchmark Results: Cost-Perf.



Benchmark Results: Energy Efficiency



Conclusions

- Most of these approaches work most of the time
  - Meaningful DSP and CPU capabilities
- Even without major DSP features, high-end CPUs can handle serious DSP tasks
- Each approach makes its own compromises
- Deciding which one to use/build is tricky