*Optimized DSP Software • Independent DSP Analysis*

# Trends and Performance in Processors for Digital Signal Processing

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## Outline

- Signal processing hardware trends: the big picture
- Processor trends
- Performance analysis
  - Comparing benchmarking approaches
  - Benchmark results for the latest processors
    - 'C64xx, SC140, 'C55xx, 'BF53x, OMAP, PXA2xx
  - How architecture affects benchmark results
  - Emerging challenges
- Conclusions

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## Processor Options Multiply

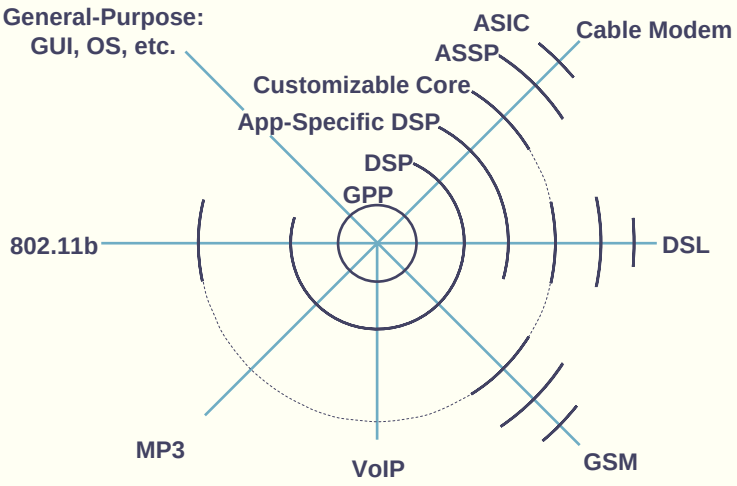
Today's system designers have a wealth of options for implementing DSP tasks:

- DSP processors
- GPPs
- Media processors
- ASSPs
- ASICs
  - Customizable cores
- FPGAs


Heterogeneous architectures increasingly common

## Flexibility vs. Suitability







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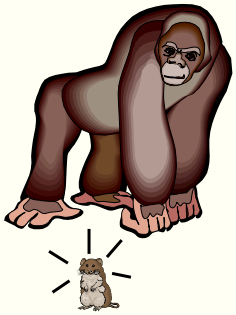
## More Options… and Fewer

More speed across the board → more options
- Many processors adding signal processing capabilities
  - E.g., ARMv6 ISA includes video-oriented instructions
- Processors stealing work from dedicated hardware
  - E.g., 'C64x can handle broadcast-quality H.264 decoding

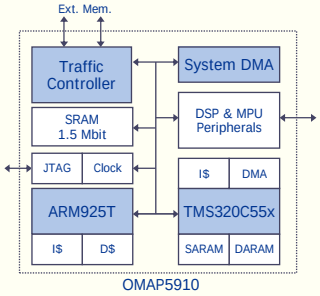
But consolidation is happening
- Faster mainstream architectures reduce need for specialized architectures
- Weak markets kill niche players
- Barriers to entry rising
  - Availability of tools, software, and programmers often crucial






## Processor Trends: Integration

Increasing integration
- More peripherals and on-chip memory
- More-powerful peripherals
- Multi-processor chips
  - Also: coprocessors
- Multi-chip packaging



OMAP5910

On-chip memory system increasingly important
- More-complex applications require more memory
- Memory speeds increase much more slowly than processor speeds
- Suitability of the memory architecture to the application is critical

## Trends: Development Support

- Applications are becoming more complex
  - Multimedia cellular phone vs. MP3 player
- Processors are becoming more complex
- Algorithms are becoming more demanding
  - And more changeable
- Optimization continues to be essential
- Huge processor-to-processor differences in development infrastructure
  - Off-the-shelf, optimized software components increasingly important
  - Software frameworks emerging

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## Processor Trends: Architecture

- VLIW (multi-issue) to increase performance
- SIMD to increase performance
- Simplified instruction sets, architectures to increase clock speeds, compilability
  - More complex instruction sets for higher performance
- Mixed-width instruction sets to reduce memory usage
- Deeper pipelines to enable higher clock speeds
- DSP-enhanced general-purpose processors
- Compatibility

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## Architecture Trends: The Down Side

- VLIW (multi-issue), SIMD, and deep pipelines can increase:
  - Memory use
  - Energy consumption
  - Code-generation complexity, programming difficulty
- Simple instruction sets often increase memory usage
  - More instructions are needed to accomplish a given task
- Complex instruction sets hinder compilability
- Compatibility can bring messy compromises

Each processor makes different tradeoffs, depending on its target application—top speed is often not the goal!

 

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## How to Benchmark?

A few candidate approaches:

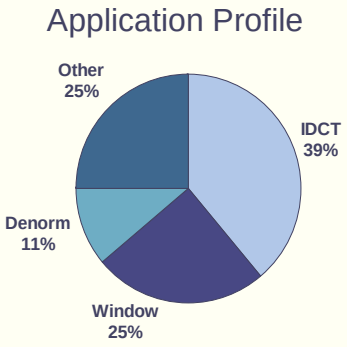
- Simplified metrics
  - E.g., MIPS (Millions of Instructions Per Second), MOPS, MMACS
- Full DSP applications
  - E.g., v.90 modem
- DSP algorithm "kernel" benchmarks
  - E.g., FIR filter, FFT




## Algorithm Kernel Benchmarks

The BDTI Benchmarks are based on DSP algorithm kernels

- The most computationally intensive portions of DSP applications
- Examples include FFTs, IIR filters, and Viterbi decoders




Benchmark results are used with application profiling to predict overall performance

## Algorithm Kernel Benchmarks

Advantages:

- Relevant; chosen by analysis of real DSP apps
- Kernels are short, allowing
  - Functionality to be precisely specified
  - Benchmarks to be implemented, optimized in a reasonable amount of time

Disadvantages:

- Not practical to implement all important algorithms
- Don't reflect application-level optimizations and trade-offs
- Ignores system-level considerations

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## Benchmark Results for the Latest Processors

High-performance processors
- Texas Instruments TMS320C64xx
- StarCore SC140

Low-power processors
- Texas Instruments TMS320C55xx
- Analog Devices Blackfin (ADSP-BF53x)

General-purpose/DSP processors
- Intel PXA2xx
- Texas Instruments OMAP5910


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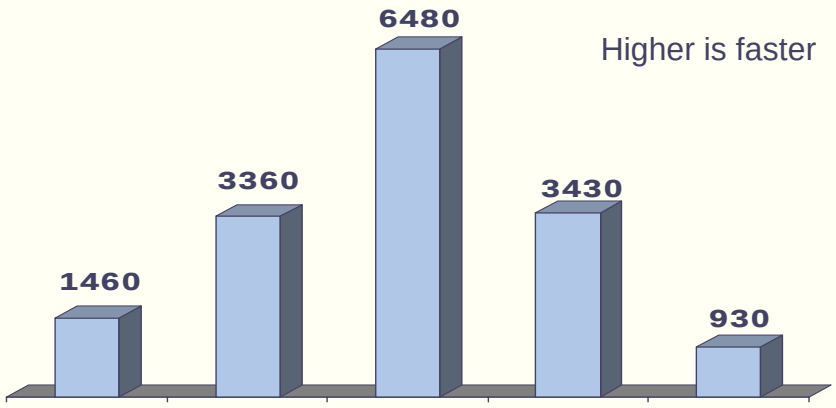
## Overall DSP Speed: BDTImark2000™





(See www.BDTI.com for more scores)
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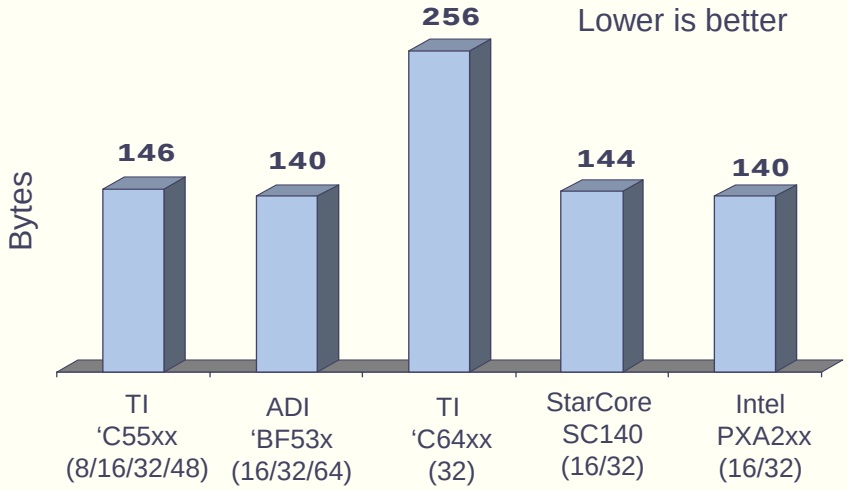
## What Factors Affect DSP Speed?

Processors' DSP speeds are affected by:

- Parallelism
  - How many parallel operations can be executed per cycle
- Instruction set
  - Suitability for the task at hand
- Clock speed
- Data types
- Data bandwidth
- Pipeline depth
  - Instruction latencies
- Support for DSP-oriented features, e.g.,
  - DSP addressing modes
  - Zero-overhead looping
  - Saturation, scaling, rounding




## Memory Use: BDTI Control Benchmark



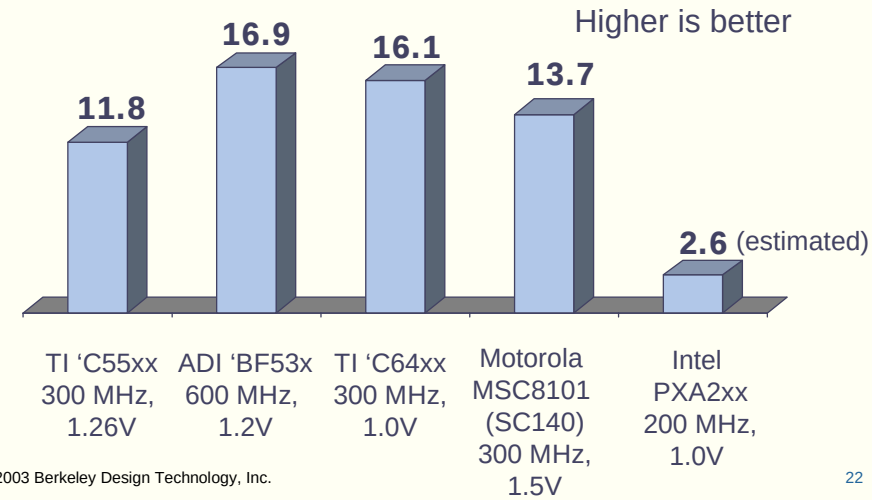
## What Factors Affect Memory Use?

Processors' memory usage affected by:

- Instruction set
  - Wider instructions take more memory
  - Mixed-width instruction sets becoming popular
    - Use short, simple instructions for simple tasks
    - Use longer instructions for more complex tasks
  - Suitability of instruction set for task at hand
- Architecture
  - VLIW, SIMD, and deep pipelines all may encourage (or require) optimizations that increase memory use to obtain speed-optimized code
- Compiler quality (for compiled code)




## Energy Efficiency: BDTImark2000/mW



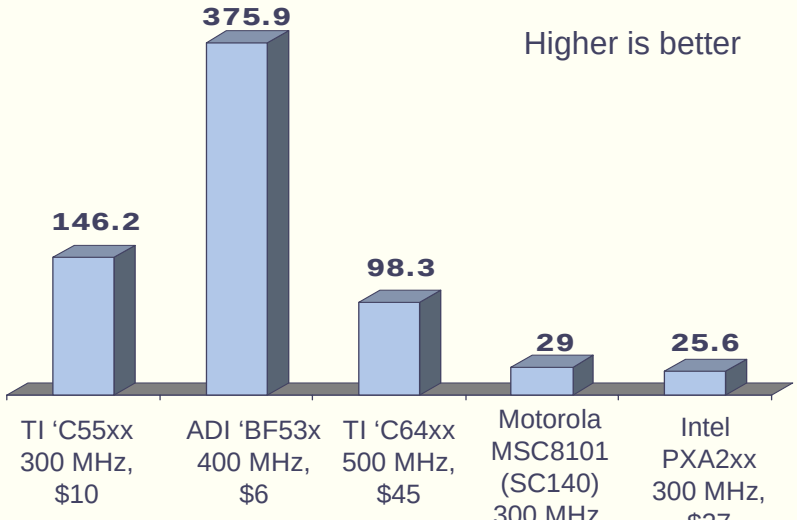
## What Factors Affect Energy Efficiency?

Processors' energy consumption affected by:

- Speed
- Hardware implementation
  - Fabrication process, **voltage**, circuit design, logic design
- Memory usage
- Compiler quality (for compiled code)




## Cost-Perf: BDTImark2000/$



## What Factors Affect Cost-Perf?

Speed

Chip cost, which is affected by:

- Die size
  - Fabrication process
  - Size of on-chip memory
    - Influenced by processor's memory usage
  - On-chip peripherals
  - Manufacturing volume

Good cost-performance results don't necessarily mean chip is suitable for apps with severe cost constraints

- Users don't want to pay for more performance than needed

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## Texas Instruments TMS320C64xx

Targets high-performance DSP applications.

Goals:

Fast
Compilable
Compatible with earlier 'C62xx

Sacrifices:

High memory consumption
High chip price for fastest ($199, qty 10K)
Difficult to program in assembly language

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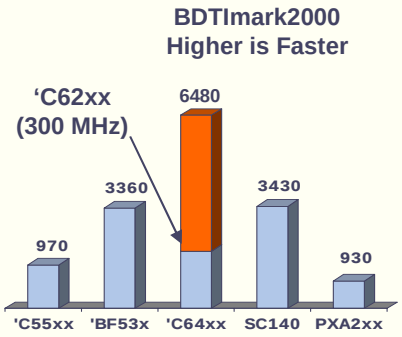
## 'C64xx is Fast Because…

Highly parallel architecture
- Based on 'C62xx: VLIW, up to 8 instructions/cycle
- Adds SIMD to 'C62xx
  - Compatible with 'C62xx
  - Faster
  - More powerful instructions
  - Four 16-bit MACs/cycle

Very high clock speed (720 MHz)
- Deep pipeline (11 stages)
- Most instructions are simple
  - 32-bit, mostly RISC-like
  - Also increases compilability
- Cache

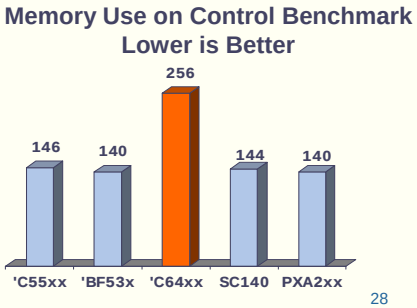






## But 'C64xx Makes Sacrifices

- High memory use
  - Wide, uniform-width (32-bit) instructions
  - Mostly simple, RISC-like instructions
  - VLIW, SIMD, deep pipeline
- Memory use increases chip/system cost
- Deep pipeline also complicates code generation
  - Multi-cycle latencies



## StarCore SC140

Targets high-performance DSP applications.

Goals:

- Fast
- Low memory usage
- Easy to program in assembly
- Compilable
- Low energy consumption

Sacrifices:

- Not as fast as 'C64xx
- High chip price (300 MHz MSC8101 is $118, qty 10K)
- No compatibility with previous architectures

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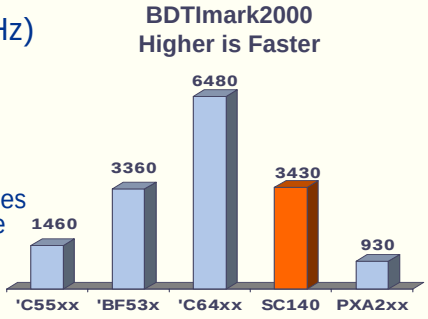
## SC140 Fast, But Not Fastest

Like 'C64xx, highly parallel architecture

- VLIW, up to 6 instructions/cycle
  - Like 'C64xx, four 16-bit MACs/cycle
- Limited SIMD

Mid-range clock speed (300 MHz)

- About half as high as 'C64xx
- Shallow pipeline (5 stages)
  - Not deep enough for ultrahigh clock speed
  - But uniform single-cycle latencies ease code generation, decrease memory use
- Simple instruction set

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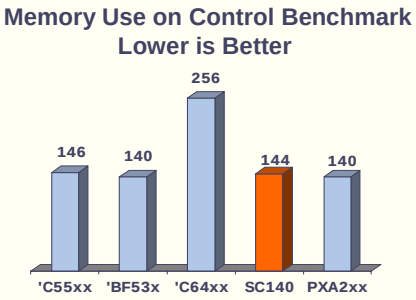
## SC140 Has Surprisingly Low Memory Use

- Mixed-width instruction set
  - 16-bit instructions with optional 16-bit prefixes
- Surprising, since it's VLIW







## Texas Instruments TMS320C55xx

Targets low-power, cost-sensitive DSP applications.

Goals:

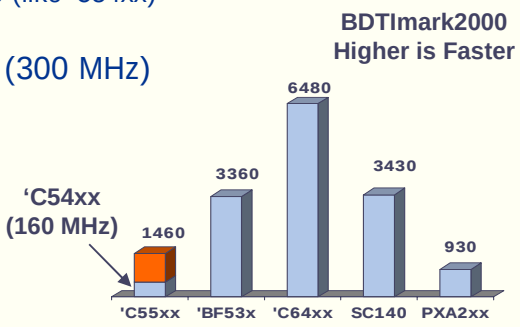
- Low energy consumption
- Low memory use
- Low chip cost
- Midrange speed
- Partly compatible with earlier 'C54xx architecture

Sacrifices:

- Not nearly as fast as high-end DSPs
- Not very compilable
- Difficult to program in assembly

## 'C55xx Focuses on Power, Cost, Compatibility... Not Speed

- Moderate parallelism
  - Adds limited (2-issue) VLIW capabilities to boost speed while maintaining partial compatibility with 'C54xx
    - Two MACs/cycle
  - Convoluted architecture (like 'C54xx)
- Moderate clock speed (300 MHz)
  - 7-stage pipeline
  - Single-cycle latencies
- Moderate price ($8-20 qty 10K)







## Analog Devices ADSP-BF53x

Targets low-power, cost-sensitive DSP applications.

Goals:

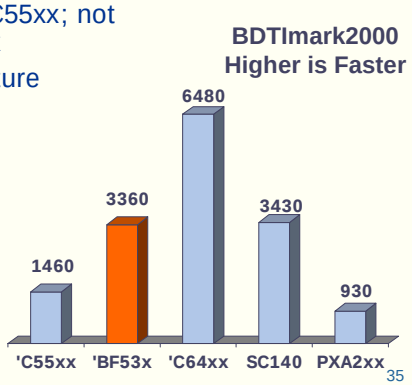
- Low energy consumption
- Low memory use
- Low chip cost
- Midrange speed
- Compilable

Sacrifices:

- Not nearly as fast as high-end DSPs
- No compatibility with previous architectures

## ADSP-BF53x Balances Power, Cost, Speed

- Moderate parallelism
  - 3-issue VLIW
    - Two MACs per cycle
  - Somewhat more parallelism than 'C55xx; not nearly as much as SC140 or 'C64xx
  - Not constrained by legacy architecture
- High clock speed (600 MHz)
  - 10-stage pipeline
  - Single-cycle latencies
- Good energy efficiency
- Moderate price ($6-35 qty 10K)

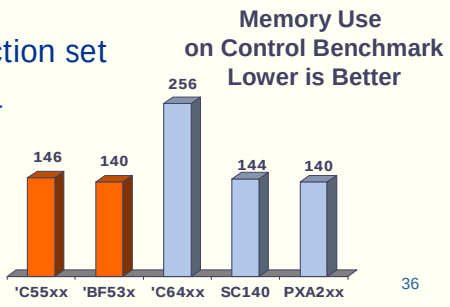






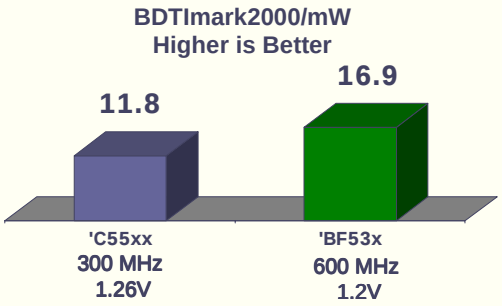
## 'BF53x and 'C55xx Both Have Low Memory Usage

- Both use mixed-width instruction sets
  - 'BF53x uses 16/32/64-bit instructions
  - 'C55xx uses instructions ranging from 8-48 bits
- 'BF53x instructions (and architecture) are fairly simple
  - 'BF53x is easy to program in assembly, good compiler target
- 'C55xx inherits 'C54xx instruction set
  - Not as easy to program in assembly as 'BF53x, but familiar to 'C54xx programmers
  - Not a good compiler target
  - Results for compiled code would likely favor 'BF53x



## 'BF53x vs. 'C55xx Energy Efficiency

- 'BF53x supports multiple voltages
  - Good energy efficiency at top speed of 600 MHz/1.2V
  - Energy results at other speed/voltage combos will vary
- 'C55xx supports one voltage







## Intel PXA2xx (XScale)

Targets low-power, cost-sensitive DSP applications where general-purpose processing features or software are needed.

Goals:

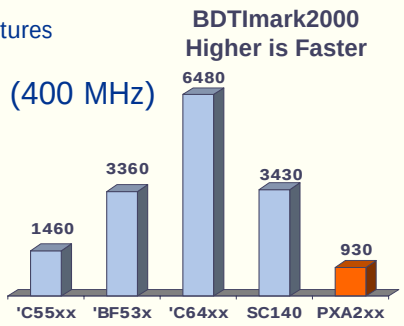
- Low memory use
- Low chip cost
- Midrange speed
- Compatible with earlier ARM architectures
- Support for operating systems, compilers

Sacrifices:

- Not very efficient for DSP
- Poor energy and cost efficiency

## PXA2xx Speed Comes from Clock

- Relatively low level of parallelism
  - Single-issue, mostly general-purpose 32-bit architecture
    - Good compiler target
  - ARM architecture augmented with limited SIMD
    - Two MACs/cycle
    - Few additional DSP-specific features
- Moderately high clock speed (400 MHz)
  - 7-stage pipeline
  - Multi-cycle latencies
- Medium-high price ($27-42 qty 10K)

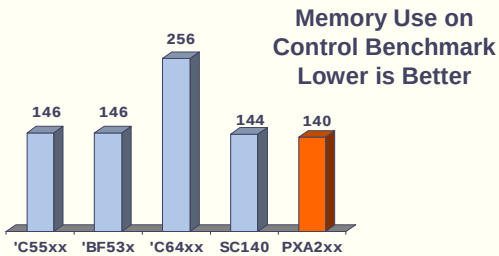






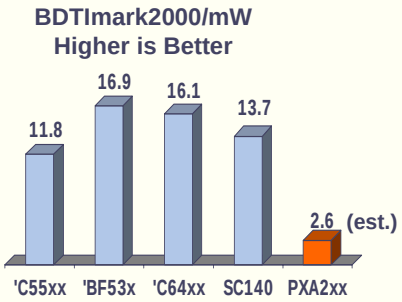
## PXA2xx is Efficient in Memory

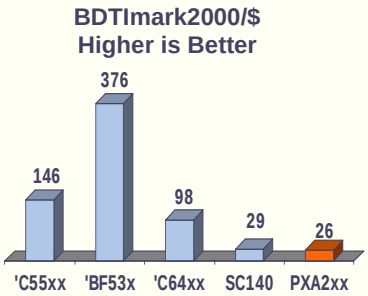
- Not surprising; general-purpose architecture is a good match for control code
- Mixed-width (16/32) instruction set
- Probably would look even better if benchmark showed compiled code results



## PXA2xx Can't Compete With DSPs on Energy, Cost

- Not very efficient on DSP algorithms
- High clock rate helps boost speed, but doesn't help with energy or chip cost
  - This is often a drawback of GPPs for DSP







## TI OMAP ('C55xx plus ARM9)

Targets low-power, cost-sensitive DSP applications where general-purpose processing features or software are needed.

Goals:

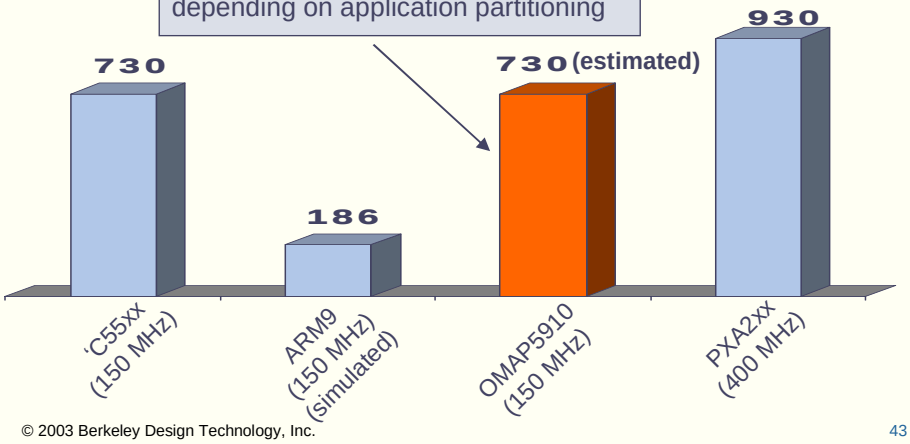
- Low energy consumption
- Low memory use
- Low chip cost
- Midrange speed
- Support for operating systems, compilers
- Compatibility with 'C54xx, ARM


Sacrifices:

- 'C55xx not very compilable
- Dual-core approach complicates system development

## OMAP BDTImark2000 Score??

OMAP5910 BDTImark2000 score could range from **186** (ARM only) to **916** (ARM plus C55xx)… depending on application partitioning







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## Emerging Benchmarking Challenges

New technologies create performance-analysis challenges
- Multi-core devices
- DSP-enhanced FPGAs
- Application-specific processors
- Customizable processors
- Reconfigurable processors

Evolving applications and tools also lead to new challenges
- Increasing reliance on C compilers




## Application Benchmarking

- For technologies not well served by kernel benchmarks, such as
  - FPGAs
  - Application-specific processors
- Limited applicability
- Practicality concerns can be partly addressed by
  - Using off-the-shelf implementations where available, or
  - Using simplified applications
    - E.g., BDTI's OFDM benchmark—simplified telecom receiver

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## Conclusions

- DSP processor architecture innovation has accelerated greatly
- New processor types are increasingly competitive
  - DSP-enhanced general-purpose processors
  - Multiprocessor chips
  - Customizable cores
- Non-processor approaches are increasingly competitive
  - DSP-enhanced FPGAs

-> Architectural options are expanding

## Conclusions

- Today's DSP-oriented processors cannot be meaningfully compared using simplified metrics
  - Relevant, meaningful benchmark results are essential to processor evaluation
- There is no ideal processor
  - Fastest doesn't mean best
    - The "best" processor depends on the details of the application
  - Different architectural approaches make different performance trade-offs
    - Understanding these is key to selecting a processor




## For More Information...

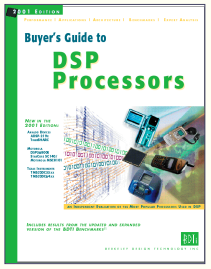
**www.BDTI.com**

Free Information
- BDTImark2000™ scores
- *DSP Insider* newsletter
- *Pocket Guide to Processors for DSP*

White papers on processor architectures and benchmarking

Article reprints on DSP-oriented processors and applications
- *EE Times*
- *IEEE Spectrum*
- *IEEE Computer* and others

*comp.dsp* FAQ

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