Selecting Application Processors for Mobile Multimedia

Presentation Goals

By the end of this workshop, you should know:

- Key selection criteria and trends for application processors
- Common approaches to multimedia acceleration used in application processors
- Key strengths and weaknesses of each approach
- Key strengths and weaknesses of representative processors from each category
Application Processors Defined

Run “user applications” in smart phones, PDAs, and other converged devices
Support mainstream OSs
  • Symbian, Windows CE, PalmOS, or Linux
Emphasize multimedia processing
  • Audio, video, still image, and 2D and 3D graphics
  • Media player, camera, games
Support Java for games and other downloaded apps
Support security features for network updates, m-commerce, DRM
Do not handle “baseband” (wireless communications)

Application vs. Baseband
Mobile Device Markets
Unit Shipment Forecast

Source: Gartner Dataquest

Application Processor Market
Application Processor Sales Forecast

Source: Forward Concepts

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Motivations for Mobile Multimedia

Add features to differentiate in a crowded market
- Examples: camera or music player in phone or PDA
Integrate features of separate products for convenience
- Examples: PDA + phone, game machine + phone
For service providers:
- Drive growth in mature markets
- Increased service revenues
- Differentiation via features

Applicaton Processor Needs

Key Considerations

Speed
- Multimedia tasks
- Multitasking
System cost
- Chip cost
- Memory use
- Integration
Size and integration
- Memory integration
- Interfaces for LCD, camera, flash, baseband processor, many others
Energy efficiency

Roadmap
- Flexibility, expandability
  - Performance headroom
  - Open software environment
    - Operating systems
    - Java
Application development
- Compatibility
- Multi-vendor support
- Tools and support
- Off-the-shelf software
- Reference designs
- Services
## Processor Vendors

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<td>TI</td>
<td>OMAP families of application, application/baseband processors</td>
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## Algorithm Kernel Benchmarks

The BDTI Benchmarks™ are based on signal-processing algorithm kernels:
- DSP algorithm kernels are the most computationally intensive portions of DSP applications.
- Example algorithm kernels include FFTs, IIR filters, and Viterbi decoders.
- Application-relevant algorithm kernels are strong predictors of overall performance.
**Benchmarking Challenges**

Algorithm kernel benchmarks are good for measuring general signal-processing performance, but they ...
- Require careful application for multi-core processors
- Cannot be easily applied to hardware accelerators
- Do not measure OS overhead
- Do not measure system-level performance

Solution: application-level benchmarks?

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**Full-Application Benchmarks**

Applications tend to be ill-defined

Hand-optimization needed
- Costly, time-consuming to implement
- Measures programmer as much as processor

Measures *system*, not just processor
- Sometimes this is an advantage

Results useful only for specific application (or similar applications)

For processors, similar results via simpler approach
- But this is not true for all implementation technologies
Selecting Application Processors for Mobile Multimedia

**Benchmark Results**

*Application Processor Median*

- **BDTImark2000™**
  - Energy Use: 1
  - Memory Use: 1
  - 10 ku Price: 1

**Multimedia Acceleration**

- **Hard-wired Accelerator(s)**
- **Programmable Coprocessor(s)**
- **DSP(s)**
- **DSP-Oriented ISA Enhancements**
  - None

*Fixed Function* → *Fully Programmable*

**Generality**
No Multimedia Acceleration
Strengths and Weaknesses

- Weak DSP performance
- Simple programming model
- Dynamic features complicate programming
  - Complicate optimization and ensuring real-time performance
  - Memory architecture is frequently a weak link
- Good tools, some with DSP support
- Mature architectures, stable roadmaps
- Multi-vendor architectures
- Very good third-party software support
- Very good compatibility

Samsung S3C24xx

Based on ARM9 core
- No DSP-specific features
- Multiplier has data-dependant throughput

32 Kbytes of cache, but no SRAM
S3C2410 multi-chip package integrates 32 MB SDRAM, 32 MB flash
- Shipping at 266 MHz, 2.0 V
- Pricing starts at $11 (10 ku) for 203 MHz version
S3C2440 sampling at 533 MHz, 1.3 V
- Pricing starts at $16 (10 ku) for 300 MHz version
MPEG-4 decode (simple profile, level 1, QCIF, 15 fps): 10-20 MHz (BDTI estimate)
S3C2410 On-Chip Integration

Samsung S3C24xx

Strengths and Weaknesses

- Moderate DSP speed
  - No DSP features; performance comes mainly from high clock rates
  - Inexpensive and cost-efficient*

- All on-chip memories are caches
  - Large stacked SRAM and flash memories on some family members

- Simple, uniprocessor architecture

- Extensive compiler, OS, and 3rd-party support

- Excellent compatibility

* Based on initial pricing provided by Samsung
DSP-Oriented ISA Enhancements

Strengths and Weaknesses

Moderate DSP performance

- Simple programming model
- Dynamic features complicate programming
  - Complicate optimization and ensuring real-time performance
  - Memory architecture is frequently a weak link
- Good tools, some with DSP support
- Some mature architectures, stable roadmaps
- Some multi-vendor architectures
- Some have very good third-party software support
- Good compatibility
  - ISA enhancements reduce compatibility

ARM ARM9E

The ARM9 Gets Modest DSP Extensions

Faster, wider multiplier hardware

- Multiply throughput no longer data-dependent
- Most 16-bit MAC operations have single-cycle throughput

Improved support for 16-bit data

- New multiply instructions treat 32-bit registers as two 16-bit values
- ALU can access register halves via “free” shifts

No DSP-oriented addressing

Targets 250 MHz in 0.13 µm

- Fabricated by LSI Logic at 200 MHz in 0.18 µm

Claim: MPEG-4 decode (simple profile, level 1, QCIF, 15 fps): 10-20 MHz
ARM ARM9E
Strengths and Weaknesses

- Moderate speed and energy-efficiency
  - No DSP addressing, parallel moves, or hardware loops
  - Conditional execution of most instructions
  - All results 32 bits wide
- Compatible with other ARM cores
- Extensive 3rd-party support
- Multi-vendor support
- Simple architecture
- Uniprocessor

ARM ARM11

New multimedia instructions
- SIMD dual-16-bit MAC, add, and subtract
- Sum-of-absolute-differences instruction for video
Other DSP-friendly features inherited from ARM10
- Branch prediction
  - Enables near-zero-overhead loops
- Parallel load/store unit and 64-bit bus
  - Limited parallel move support
  - Reduced memory bottleneck
Java acceleration and optional floating-point unit
8-stage pipeline
Targets 400 MHz in 0.13 µm
Intel PXA2xx (XScale Based)

XScale implements ARMv5TE instruction set, but adds:
- SIMD dual-16-bit MAC
- SIMD dual-16-bit add and/or subtract
- 40-bit accumulator

XScale microarchitecture differs from ARM cores
- Longer pipeline: 7 stages vs. 5 stages
- Adds branch prediction

PXA2xx includes 66 Kbytes of cache, but no SRAM
PXA26x “stacked” with flash

Speed/voltage scaling: 400 MHz/1.3 V to 200 MHz/1.0 V
Shipping at 400 MHz, $36 (10 ku)

MPEG-4 decode (simple profile, level 1, QCIF, 15 fps): 10-20 MHz (BDTI estimate)

PXA255 On-Chip Integration

- Real Time Clock
- Timer/PWM
- AC97
- I²S
- I²C
- IrDA/UART
- SSP/SPI/uWire
- MMC/SD
- UART
- Bluetooth UART
- USB 1.1
- GPIO
- JTAG
- DMA
- Color LCD Controller
- Interrupt Controller
- PCMCIA/CF Card Control
- Burst Flash Interface
- Variable Latency I/O
- SDRAM Control
- Address & 16/32 Data Mux
- SRAM Control

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Intel PXA2xx

**Strengths and Weaknesses**

- **Good speed**
- Most family members are expensive
  - Large stacked flash memories on most family members may offset cost
- Moderate cost- and energy-efficiency
  - Few DSP features; performance comes mainly from high clock rates
  - Unusual speed/energy flexibility
- Good memory efficiency
- Good OS and compiler support
- All on-chip memories are caches
  - Mini data cache reduces cache thrashing

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Intel Wireless MMX

64-bit SIMD extensions to XScale

- Eight 8-bit, four 16-bit, two 32-bit, or one 64-bit operation per instruction
- Superset of x86 MMX and integer SSE operations
- Provides porting path from desktop x86 applications
  - But x86-optimized software will require substantial re-optimization

Unusually large (sixteen 64-bit registers) register file
- Increases performance, reduces energy consumption

No special instructions for wireless communications
No changes to buses, addressing, ...
No products announced yet
DSP(s)

Strengths and Weaknesses

- Enough signal-processing speed for most tasks
- But insufficient for cutting-edge tasks
- Architecture designed for signal-processing
  - Eases optimization, ensuring real-time behavior
  - Improved energy efficiency
- Improved task-switching efficiency, responsiveness
- Complex (multiprocessor) programming model
- Generally good tools with signal-processing features
- Good third-party software component support
- Good compatibility for some
- Some mature architectures, stable roadmaps
- No multi-vendor architectures

Texas Instruments OMAP5910

150 MHz ARM9 core
- 32-bit multiplier with data-dependant throughput

150 MHz ‘C55x core
- Up to two 16-bit MACs per cycle
- Accelerators for video, imaging

Cores interact via mailbox registers, shared memory, and DMA transfers
320 Kbytes of on-chip cache and SRAM

Extensive development support, including GPP-DSP API, multi-core-aware tools

Excellent 3rd-party software support
Claim: MPEG-4 decode (simple profile, level 1, QCIF, 15 fps): 10-15 MHz
Sampling at $25 (10 ku)
Texas Instruments OMAP5910

Strengths and Weaknesses

**Strengths:**
- Good speed and energy-and cost-efficiency from 'C55x core
- Image, video accelerators boost performance
- Memory system designed for signal processing
- Both cores well established
  - Strong tools, 3rd-party software support
  - Design-house network
- Dual-core architecture complicates programming
  - But may improve responsiveness
  - Careful application partitioning critical

**Weaknesses:**
- Dual-core architecture complicates programming
- Careful application partitioning critical

Programmable Coprocessor(s)

Strengths and Weaknesses

**Strengths:**
- Architecture designed for media processing
  - Potential for strong performance
  - Potential for good energy efficiency
  - May rely on GPP core for media “glue logic”
- Complex, unique, unfamiliar programming models
  - Tools generally immature
- Very limited third-party software component support
- Flexibility may be limited by architecture or by programming complexity
- No multi-vendor architectures
- Little compatibility

**Weaknesses:**
- Complex, unique, unfamiliar programming models
- Tools generally immature
- Very limited third-party software component support
- Flexibility may be limited by architecture or by programming complexity
- No multi-vendor architectures
- Little compatibility
NeoMagic MiMagic 6

200 MHz ARM9E core, plus ...
Fixed-function accelerators for simple tasks
  - BitBlt, color space conversion, scaling, ...
"Associative Processing Array" programmable coprocessor for complex tasks
  - Video, 3-D graphics
Extensive I/O interfaces
  - Direct connection to camera sensor, LCD, ...
  - Dedicated interface for baseband processor
Claim: MPEG-4 decode (simple profile, level 1, QCIF, 15 fps): 13 MHz
Sampling third quarter 2003, $18 (10 ku)
**Associative Processing Array**

Array of 1-bit memory and processing elements
- Serves as both processing engine and as cache
- First implementation: 512 rows x 160 columns

Operations performed column-wise
- Operations performed on 512 rows in parallel

Only three basic operations: compare, write, move
- Complex operations built up via Boolean logic
- E.g., 8-bit addition requires 25 cycles
  - But can do 512 at once → throughput ~20 per cycle

Common word-wise operations supported via library

**NeoMagic MiMagic 6**

**Strengths and Weaknesses**

- Performance, efficiency unknown
- Exemplary integration
  - Designed from the ground up for multimedia
- APA may deliver excellent energy efficiency
  - Potential for dramatic reduction in data movement
- 3D graphics acceleration
- APA is programmable, and therefore flexible, but ...
- Very unusual, complex programming model
  - NeoMagic will provide a few key software blocks
  - For other functions, users must brave a complex architecture with immature tools
Hard-wired Accelerator(s)

Strengths and Weaknesses

► Architecture designed for media processing
  ▲ Potential for excellent speed and energy efficiency
  ▼ Typically perform well only on a narrow set of tasks
  ▼ Limited scope of typical hardwired accelerators may require GPP to handle significant media processing loads
  ▼ Limited flexibility

► Simple programming model
  ▼ No multi-vendor architectures
  ▼ Little compatibility
  ▼ Limited third-party software component support

MediaQ MQ9xxx (Katana)

Based on 144 MHz ARM9
Accelerators for video, JPEG encode, 2D graphics, and Java
Unusually large on-chip SRAM (320-480 Kbytes)
Video input port
Strong emphasis on energy-saving design
  ▪ Accelerators to reduce overall clock speed
  ▪ Independent clock speeds for each module
  ▪ Aggressive clock gating, fast wake-up
MPEG-4 decode (simple profile, level 1, QCIF, 15 fps): 10-20 MHz (BDTI estimate)
First family member sampling now at $14 (10 ku)
MediaQ MQ9xxx (Katana)
Chip-Level Architecture

MQ9100/9150
- Bus Interface
- ARM922 CPU
- Java Engine
- 480 Kbytes eSRAM
- JPEG Encode
- Video Proc.
- Video Input
- UART
- UART
- SDIO
- USB 1.1
- AC97/12S
- SPI
- KMI
- Flat Panel Interface
- Flat Panel Interface
- Main LCD
- Sub LCD
- Keypad
- IRDA
- VGA/MPixel
- Bluetooth
- 802.11/WAN
- Flat Panel Interface
- Flash/DOC
- SDRAM
- NAND
- 16 32 8

MediaQ MQ9xxx (Katana)
Strengths and Weaknesses

* Potential for good energy-efficiency for some tasks
  * Limited by lack of video decompression acceleration

* Low cost and large on-chip SRAM

* Potential for good performance, cost-performance
  * Likely good speed for targeted tasks

* Relatively inflexible

* Potentially simple programming model
  * Fixed-function accelerators require little low-level programming

* Vendor has experience in related applications
Related Markets and Processors

Integrated application/baseband processors
- OMAP730, MSM7xxx

Feature phone processors
- OMAP3xx, SoftFone

Consumer media processors
- Blackfin, DSC2x, DMxxx

Telematics processors
- Blackfin, SH-4, ST100, TriCore

Example: Intel PXA800F

Dual-core chip:
- 312 MHz XScale core
- 104 MHz MSA core

Contains embedded Flash
- Enables wide memory buses; MSA Flash interface is 64-bit
- Low-latency access

Cores, Flash operate at 1.2 V

Targets “feature phones” running an RTOS
Sampling at $35 (10 ku)
Applications Processors Trends

New apps move to the fore
  • 3D games
  • Personal content

Increasing architectural complexity
  • Many heterogeneous multiprocessors
  • More specialized accelerators

Hardware abstraction increases
  • OSs, drivers, APIs, ...
  • Vendor-provided libraries

Integration increasing
  • Memory integration particularly important

Flexibility vs. efficiency is a key dilemma

Future Multimedia Applications

Convergence and Personal Content

Faster processors enable inexpensive combination of multimedia capabilities with other functions
  • Added to devices like phones and PDAs
  • Enabling new products like A/V jukeboxes and media servers

“Personal content” changes everything
  • Access media anytime, anywhere, anyway
  • Content freed from hardware
  • Connectivity becomes a key challenge

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Conclusions

Emerging mobile applications make increasingly tough signal-processing demands

- Many architectural approaches can get the job done, but efficiency, ease of development, etc. vary widely
- Serious DSP-oriented features appearing in even low-end processors

Performance comparisons become increasingly difficult as applications converge and architectures diverge

- Independent benchmarking a must

Raw performance is not enough

- Considerations like development infrastructure and vendor roadmap are crucial

For More Information...

www.BDTI.com

Free Information

- BDTImark2000™ scores
- DSP Insider newsletter
- Pocket Guide to Processors for DSP

White papers on processor architectures and benchmarking

Article reprints on DSP-oriented processors and applications

- EE Times
- IEEE Spectrum
- IEEE Computer and others
- comp.dsp FAQ