


DSP Benchmark Results for the Latest Processors

Optimized DSP Software • Independent DSP Analysis




DSP Benchmark Results for the Latest Processors (Workshop 427)

Berkeley Design Technology, Inc.
2107 Dwight Way, Second Floor
Berkeley, California 94704
USA
+1 (510) 665-1600

info@BDTI.com
<http://www.BDTI.com>

© 2003 Berkeley Design Technology, Inc.




Outline

- Why are benchmarks important?
- Comparing benchmarking approaches
- Benchmark results for the latest processors
 - 'C64xx, SC140, 'C55xx, 'BF53x, OMAP, PXA2xx
- The effect of architecture on benchmark results
 - Architectural trends and trade-offs
- Emerging challenges in benchmarking
- Conclusions

© 2003 Berkeley Design Technology, Inc. 2

© 2003 Berkeley Design Technology, Inc.




Why Benchmark?

- Assess and compare key processor metrics accurately
 - DSP speed
 - Memory efficiency
 - Energy efficiency
 - Cost-performance

- Compare performance across a wide range of architectures (conventional, VLIW, SIMD, DSP-enhanced GPP, etc.)—difficult without benchmarks
 - Simple metrics (MIPS, MACS) don't cut it

© 2003 Berkeley Design Technology, Inc. 3



How to Benchmark?


A few candidate approaches:

- Simplified metrics
 - E.g., MIPS (Millions of Instructions Per Second), MOPS, MMACS

- Full DSP applications
 - E.g., v.90 modem

- DSP algorithm “kernel” benchmarks
 - E.g., FIR filter, FFT

© 2003 Berkeley Design Technology, Inc. 4



What's Wrong with MIPS?


MIPS and MFLOPS (Millions of Floating-Point Operations per Second) are frequently used as shorthand for processor speed. But are they really meaningful?

Two instructions from different processors:

DSP16410
A0=A0+P0+P1 P0=Xh*Yh P1=XI*YI Y=*R0++ X=*PT0++

TMS320C6414
ADD A0,A3,A0

© 2003 Berkeley Design Technology, Inc. 5




Full-Application Benchmarks

This approach has pros and cons

- Applications tend to be ill-defined
- Hand-optimization needed
 - Costly, time-consuming to implement
 - Measures programmer as much as processor
- Measures *system*, not just processor
 - Sometimes this is an advantage
- Results useful only for specific app (or similar apps)
 - But if results are available for your app, this not a disadvantage
- For processors, similar results via simpler approach
 - But this is not true for all DSP implementation technologies

© 2003 Berkeley Design Technology, Inc. 6

DSP Benchmark Results for the Latest Processors



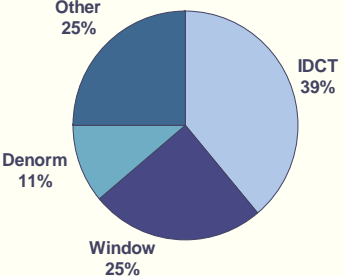
Algorithm Kernel Benchmarks

The BDTI Benchmarks are based on DSP algorithm kernels

- The most computationally intensive portions of DSP applications
- Examples include FFTs, IIR filters, and Viterbi decoders


Benchmark results are used with application profiling to predict overall performance

Application Profile



Category	Percentage
IDCT	39%
Window	25%
Other	25%
Denorm	11%

© 2003 Berkeley Design Technology, Inc. 7



Algorithm Kernel Benchmarks

Advantages:


- Relevant; chosen by analysis of real DSP apps
- Kernels are short, allowing
 - Functionality to be precisely specified
 - Benchmarks to be implemented, optimized in a reasonable amount of time

Disadvantages:

- Not practical to implement all possible algorithms
- Don't reflect application-level optimizations and trade-offs
 - For some implementation technologies, this is a problem
- Ignores system-level considerations
 - This, too, is a problem for some implementation technologies

© 2003 Berkeley Design Technology, Inc. 8

© 2003 Berkeley Design Technology, Inc.



Vendor Benchmarks


Many processor vendors provide benchmark results, but

- Benchmarks not standardized across vendors
- Results not independently verified
- Clock speeds often projected

Results are often misused, for example,

- Comparing results for functionally different benchmarks
- Comparing fastest chip to slowest from another vendor
- Comparing vaporware to real silicon
- Presenting cycle counts as a proxy for performance
- Cherry-picking benchmark results

© 2003 Berkeley Design Technology, Inc. 9



Benchmark Results for the Latest Processors

High-performance processors

- Texas Instruments TMS320C64xx
- StarCore SC140

Low-power processors

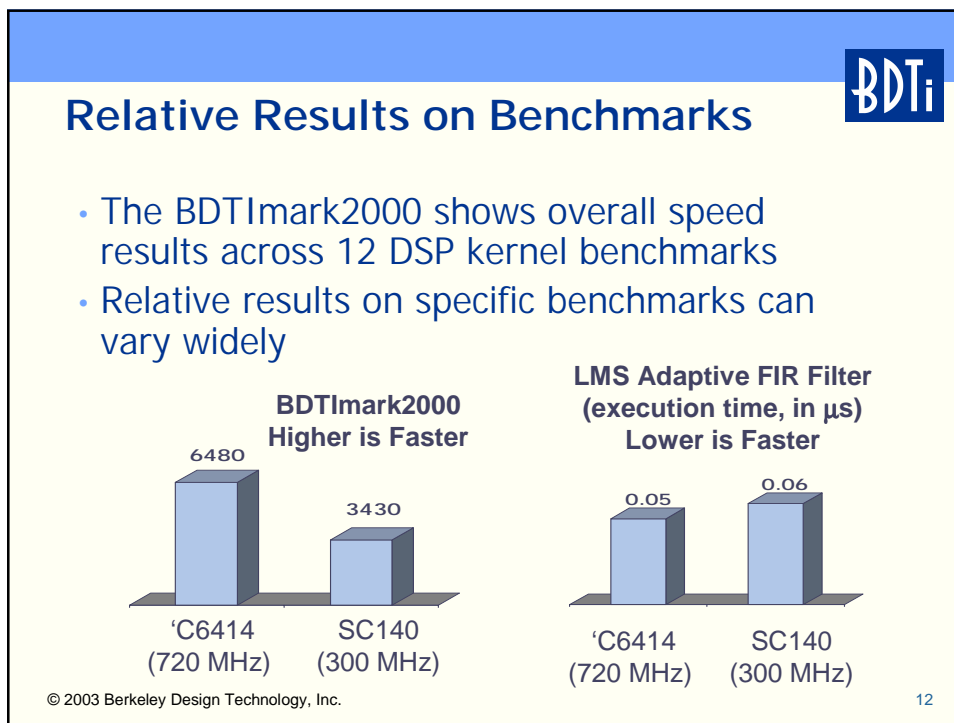
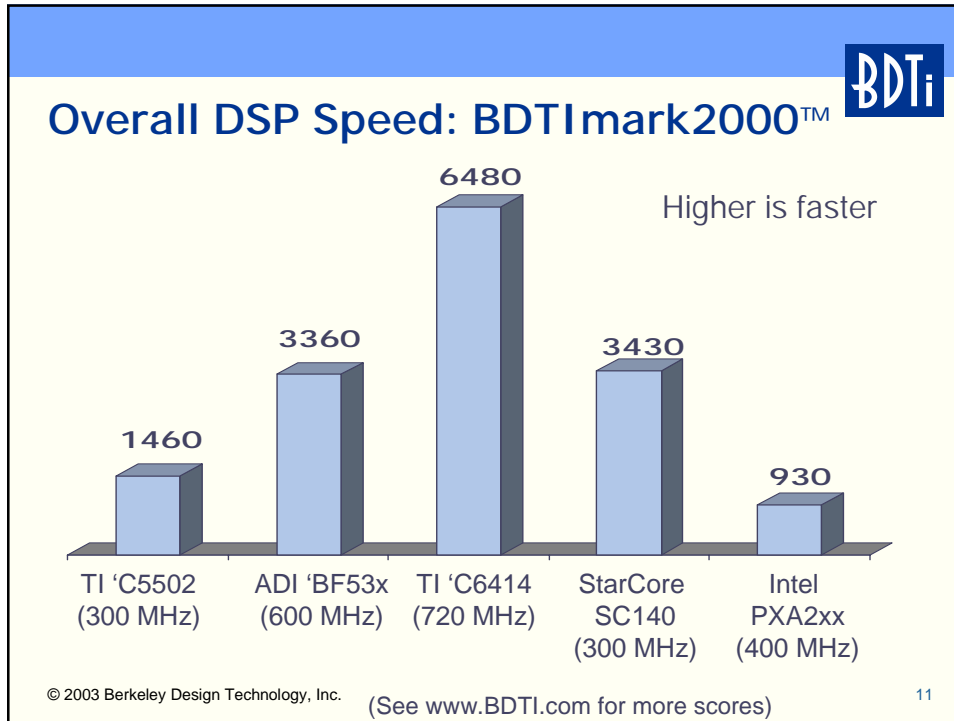
- Texas Instruments TMS320C55xx
- Analog Devices Blackfin (ADSP-BF53x)

General-purpose/DSP processors

- Intel PXA2xx
- Texas Instruments OMAP5910


© 2003 Berkeley Design Technology, Inc. 10

DSP Benchmark Results for the Latest Processors



© 2003 Berkeley Design Technology, Inc.

DSP Benchmark Results for the Latest Processors

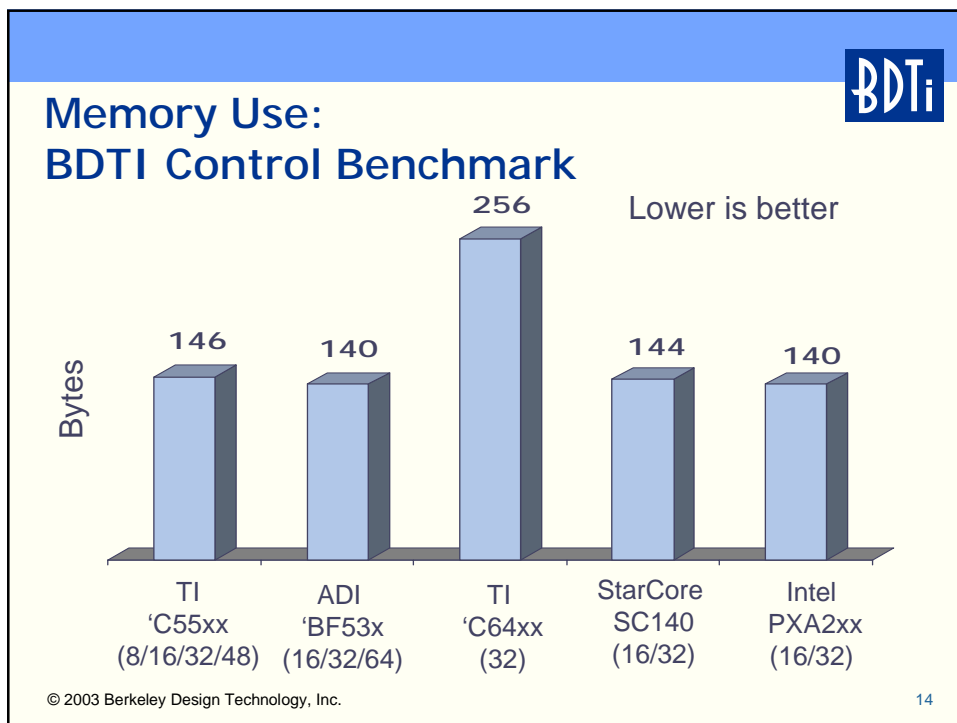


What Factors Affect DSP Speed?

Processors' DSP speeds are affected by:

- Parallelism
 - How many parallel operations can be executed per cycle
- Instruction set
 - Suitability for the task at hand
- Clock speed
- Data types
- Data bandwidth
- Pipeline depth
 - Instruction latencies
- Support for DSP-oriented features, e.g.,
 - DSP addressing modes
 - Zero-overhead looping
 - Saturation, scaling, rounding

© 2003 Berkeley Design Technology, Inc. 13



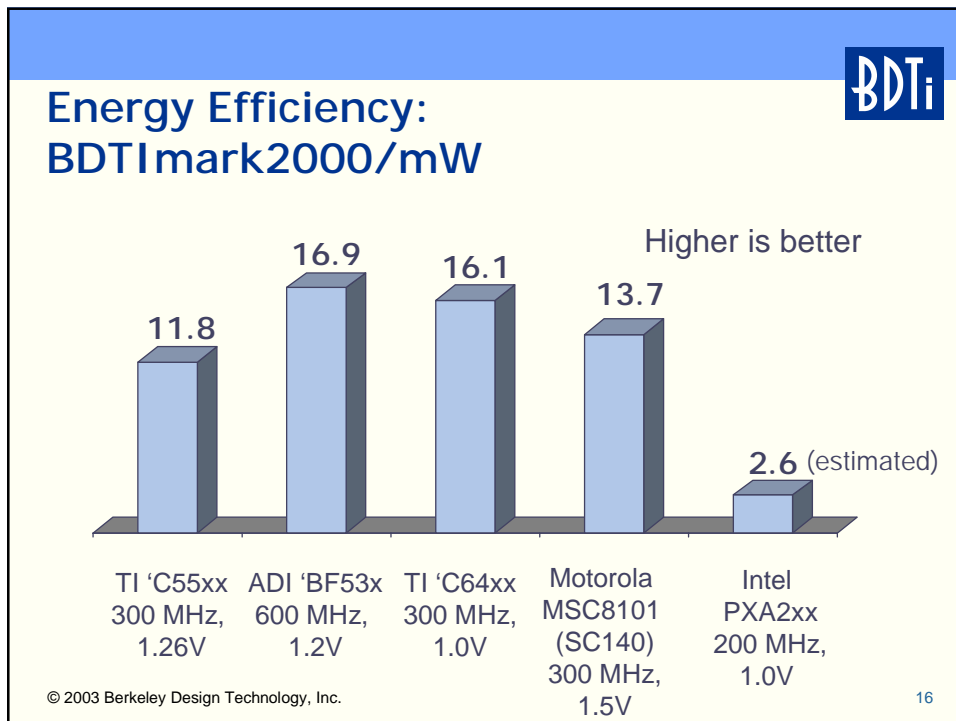
© 2003 Berkeley Design Technology, Inc.

What Factors Affect Memory Use?


Processors' memory usage affected by:

- Instruction set
 - Wider instructions take more memory
 - Mixed-width instruction sets becoming popular
 - Use short, simple instructions for simple tasks
 - Use longer instructions for more complex tasks
 - Suitability of instruction set for task at hand
- Architecture
 - VLIW, SIMD, and deep pipelines all may encourage (or require) optimizations that increase memory use to obtain speed-optimized code
- Compiler quality (for compiled code)

© 2003 Berkeley Design Technology, Inc. 15



DSP Benchmark Results for the Latest Processors

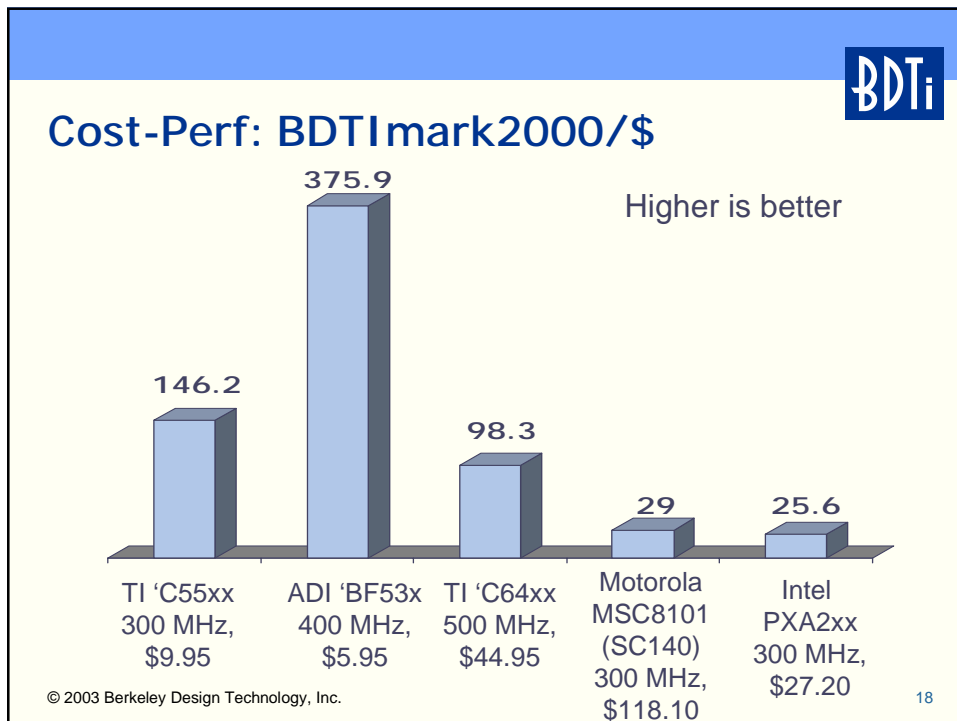


What Factors Affect Energy Efficiency?


Processors' energy consumption affected by:

- Hardware implementation
 - Fabrication process, voltage, circuit design, logic design
- Memory usage
- Match between instruction set and task at hand
- Compiler quality (for compiled code)

© 2003 Berkeley Design Technology, Inc. 17



© 2003 Berkeley Design Technology, Inc.



What Factors Affect Cost-Perf?

Speed


Chip cost, which is affected by:

- Die size
 - Fabrication process
 - Size of on-chip memory
 - Influenced by processor's memory usage
 - On-chip peripherals

Good cost-performance results don't necessarily mean chip is suitable for apps with severe cost constraints

- OEMs don't want to pay for more performance than is needed


© 2003 Berkeley Design Technology, Inc. 19



Architectural Trends

- VLIW (multi-issue) to increase performance
- SIMD to increase performance
- Simplified instruction sets, architectures to increase clock speeds, compilability
- Mixed-width instruction sets to reduce memory usage
- Deeper pipelines to enable higher clock speeds
- DSP-enhanced general-purpose processors (GPPs)

© 2003 Berkeley Design Technology, Inc. 20




Architectural Trends: The Down Side

- VLIW (multi-issue), SIMD, and deep pipelines can increase
 - Memory use
 - Energy consumption
 - Code-generation complexity
- Simple instruction sets often increase memory usage
 - More instructions are needed to accomplish a given task
- Sometimes a processor's legacy constraints are overriding

Each processor makes different tradeoffs, depending on its target application—top speed is often not the goal!

© 2003 Berkeley Design Technology, Inc. 21



Texas Instruments TMS320C64xx

Targets high-performance DSP applications.

Goals:


- Fast
- Compilable
- Compatible with earlier 'C62xx

Sacrifices:

- High memory consumption
- High chip price for fastest (\$199, qty 10K)
- Difficult to program in assembly language

© 2003 Berkeley Design Technology, Inc. 22

DSP Benchmark Results for the Latest Processors



'C64xx is Fast Because...

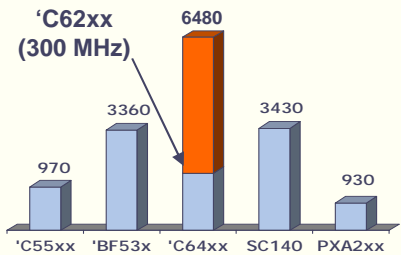
Highly parallel architecture

- Based on 'C62xx: VLIW, up to 8 instructions/cycle
- Adds SIMD to 'C62xx
 - Faster, but still compatible
 - Four 16-bit MACs/cycle
 - More powerful instructions

Very high clock speed (720 MHz)


- Deep pipe (11 stages)
- Most instructions are simple
 - 32-bit, mostly RISC-like
 - Also increases compilability
- Caching

**BDTImark2000
Higher is Faster**



Processor	BDTImark2000 Score
'C55xx	970
'C62xx (300 MHz)	3360
'C64xx	6480
SC140	3430
PXA2xx	930

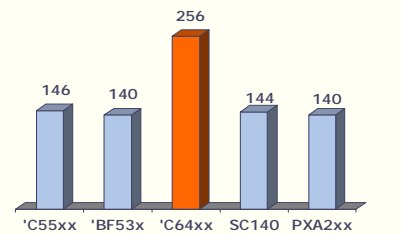
© 2003 Berkeley Design Technology, Inc. 23



But 'C64xx Makes Sacrifices

- High memory use
 - Wide, uniform-width (32-bit) instructions
 - Mostly simple, RISC-like instructions
 - VLIW, SIMD, deep pipeline
- Memory use increases chip cost
- Deep pipe also complicates code generation
 - Multi-cycle latencies


**Memory Use on Control Benchmark
Lower is Better**



Processor	Memory Use on Control Benchmark
'C55xx	146
'BF53x	140
'C64xx	256
SC140	144
PXA2xx	140

© 2003 Berkeley Design Technology, Inc. 24

DSP Benchmark Results for the Latest Processors



StarCore SC140

Targets high-performance DSP applications.


Goals:

- Fast
- Low memory usage
- Easy to program in assembly
- Compilable
- Low energy consumption

Sacrifices:

- Not as fast as 'C64xx
- High chip price (300 MHz MSC8101 is \$118, qty 10K)
- No compatibility with previous architectures

© 2003 Berkeley Design Technology, Inc. 25



SC140 Fast, But Not Fastest

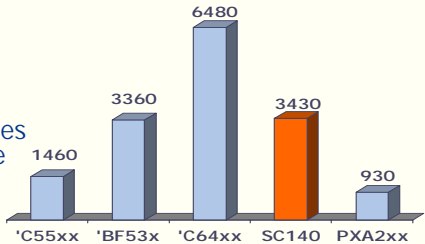
Like 'C64xx, highly parallel architecture

- VLIW, up to 6 instructions/cycle
 - Like 'C64xx, four 16-bit MACs/cycle
- Limited SIMD

Mid-range clock speed (300 MHz)

- About half as high as 'C64xx
- Shallow pipe (5 stages)
 - Not deep enough for ultrahigh clock
 - But uniform single-cycle latencies ease code generation, decrease memory use
- Simple instruction set


**BDTImark2000
Higher is Faster**



Processor	BDTImark2000 Score
'C55xx	1460
'BF53x	3360
'C64xx	6480
SC140	3430
PXA2xx	930

© 2003 Berkeley Design Technology, Inc. 26

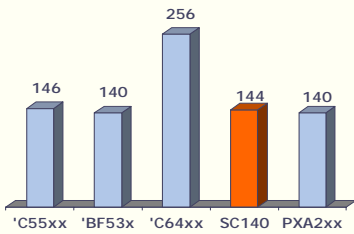
© 2003 Berkeley Design Technology, Inc.



SC140 Has Surprisingly Low Memory Use


- Mixed-width instruction set
 - 16-bit instructions with optional 16-bit prefixes
- Surprising, since it's VLIW and uses RISC-like instructions

**Memory Use on Control Benchmark
Lower is Better**



Processor	Memory Use
'C55xx	146
'BF53x	140
'C64xx	256
SC140	144
PXA2xx	140

© 2003 Berkeley Design Technology, Inc. 27



Texas Instruments TMS320C55xx

Targets low-power, cost-sensitive DSP applications.

Goals:


- Low energy consumption
- Low memory use
- Low chip cost
- Midrange speed
- Partly compatible with earlier 'C54xx architecture

Sacrifices:

- Not nearly as fast as high-end DSPs
- Not very compilable
- Difficult to program in assembly

© 2003 Berkeley Design Technology, Inc. 28

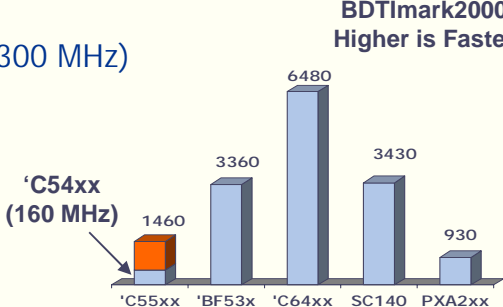
DSP Benchmark Results for the Latest Processors



'C55xx Focuses on Power, Cost, Compatibility... Not Speed


- Moderate parallelism
 - Adds limited (2-issue) VLIW capabilities to boost speed while maintaining partial compatibility with 'C54xx
 - Two MACs/cycle
 - Convoluted architecture (like 'C54xx)
- Medium clock speed (300 MHz)
 - 7-stage pipeline
 - Single-cycle latencies
- Moderately priced (\$8-20 qty 10K)

BDTImark2000
Higher is Faster



Processor	BDTImark2000 Score
'C55xx (160 MHz)	1460
'BF53x	3360
'C64xx	6480
SC140	3430
PXA2xx	930

© 2003 Berkeley Design Technology, Inc. 29



Analog Devices ADSP-BF53x

Targets low-power, cost-sensitive DSP applications.

Goals:

- Low energy consumption
- Low memory use
- Low chip cost
- Midrange speed
- Compatible


Sacrifices:

- Not nearly as fast as high-end DSPs
- No compatibility with previous architectures

© 2003 Berkeley Design Technology, Inc. 30

© 2003 Berkeley Design Technology, Inc.

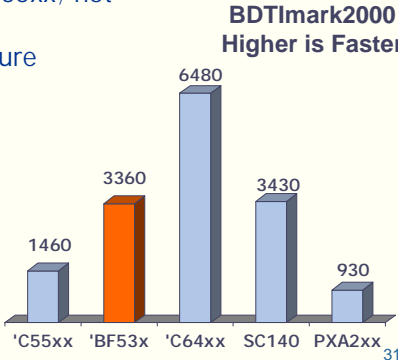
DSP Benchmark Results for the Latest Processors



ADSP-BF53x Balances Power, Cost, Speed


- Moderate parallelism
 - 3-issue VLIW
 - Two MACs per cycle
 - Somewhat more parallelism than 'C55xx; not nearly as much as SC140 or 'C64xx
 - Not constrained by legacy architecture
- High clock speed (600 MHz)
 - 10-stage pipeline
 - Single-cycle latencies
- Good energy efficiency
- Moderately priced (\$6-35 qty 10K)

**BDTImark2000
Higher is Faster**



Processor	BDTImark2000 Score
'C55xx	1460
'BF53x	3360
'C64xx	6480
SC140	3430
PXA2xx	930

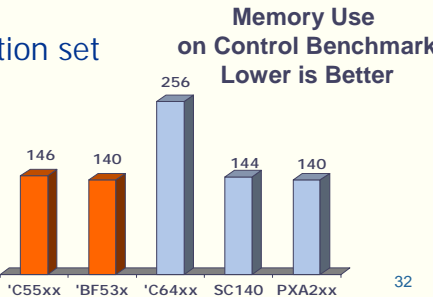
© 2003 Berkeley Design Technology, Inc. 31



'BF53x and 'C55xx Both Have Low Memory Usage

- Both use mixed-width instruction sets
 - 'BF53x uses 16/32/64-bit instructions
 - 'C55xx uses instructions ranging from 8-48 bits
- 'BF53x instructions (and architecture) are fairly simple
 - 'BF53x is easy to program in assembly, good compiler target
- 'C55xx inherits 'C54xx instruction set
 - Not as easy to program in assembly as 'BF53x, but familiar to 'C54xx programmers
 - Not a good compiler target
 - Results for compiled code would likely favor 'BF53x

**Memory Use
on Control Benchmark
Lower is Better**

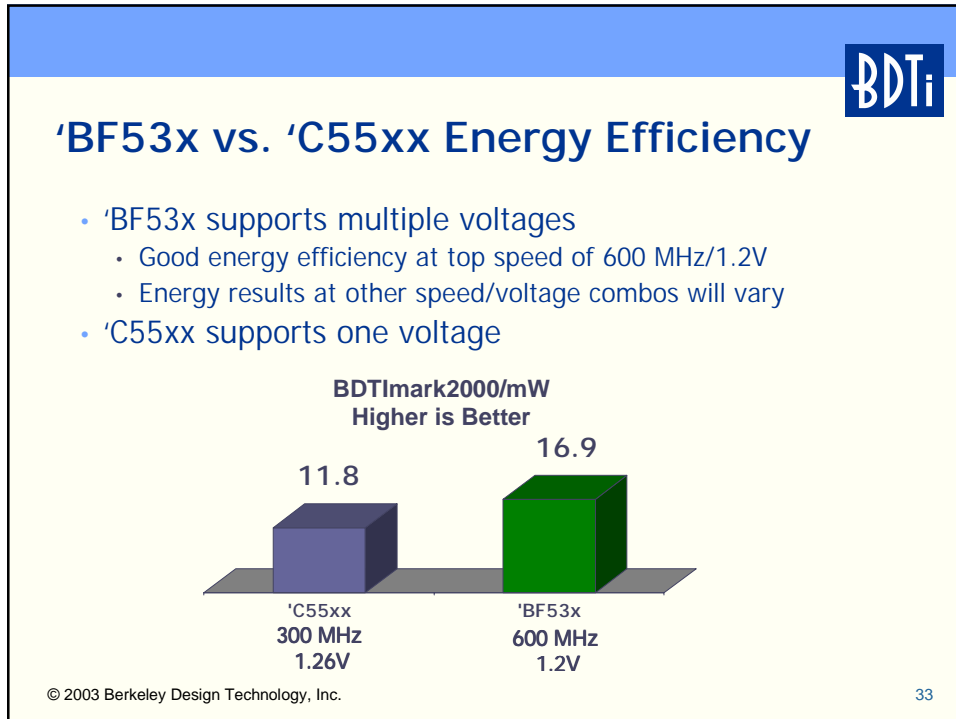


Processor	Memory Use on Control Benchmark
'C55xx	146
'BF53x	140
'C64xx	256
SC140	144
PXA2xx	140

© 2003 Berkeley Design Technology, Inc. 32

© 2003 Berkeley Design Technology, Inc.

DSP Benchmark Results for the Latest Processors



BDTi

Intel PXA2xx (XScale)

Targets low-power, cost-sensitive DSP applications where general-purpose processing features or software are needed.

Goals:

- Low memory use
- Low chip cost
- Midrange speed
- Compatible with earlier ARM architectures
- Support for operating systems, compilers

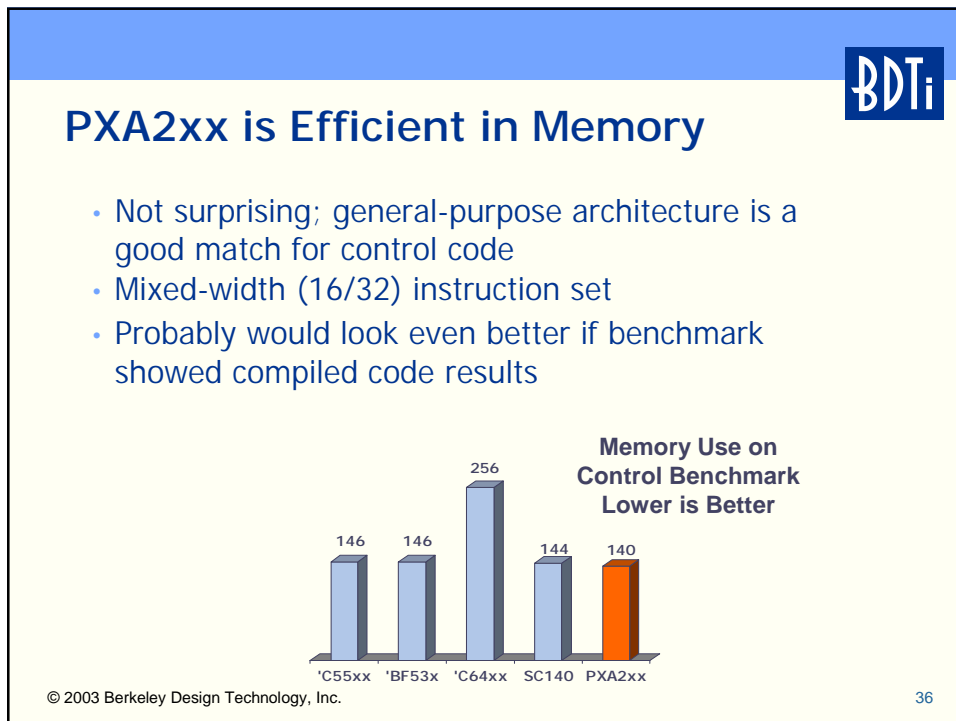
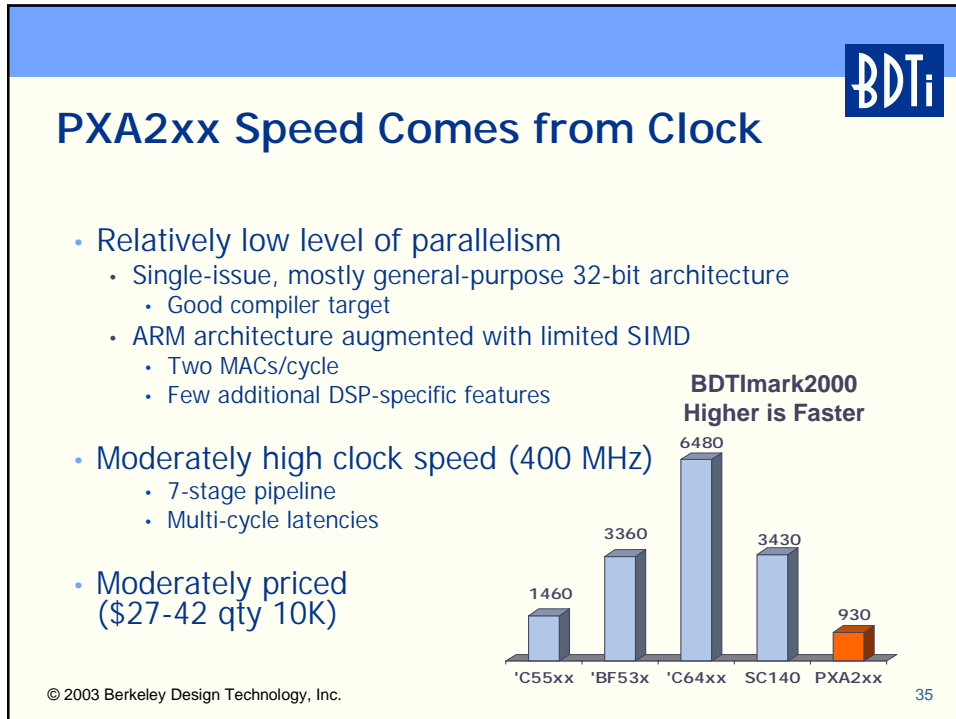
Sacrifices:

- Not very efficient for DSP
- Poor energy and cost efficiency

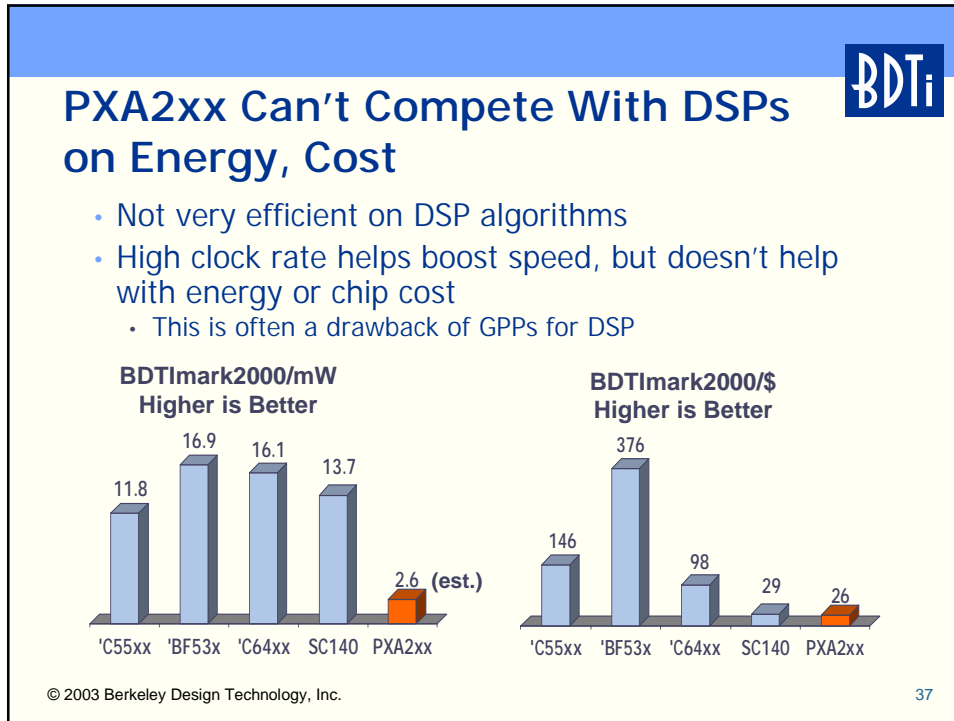
© 2003 Berkeley Design Technology, Inc. 34

© 2003 Berkeley Design Technology, Inc.

DSP Benchmark Results for the Latest Processors



© 2003 Berkeley Design Technology, Inc.




TI OMAP ('C55xx plus ARM9)

Targets low-power, cost-sensitive DSP applications where general-purpose processing features or software are needed.

Goals:

- Low energy consumption
- Low memory use
- Low chip cost
- Midrange speed
- Support for operating systems, compilers
- Compatibility with 'C54xx, ARM

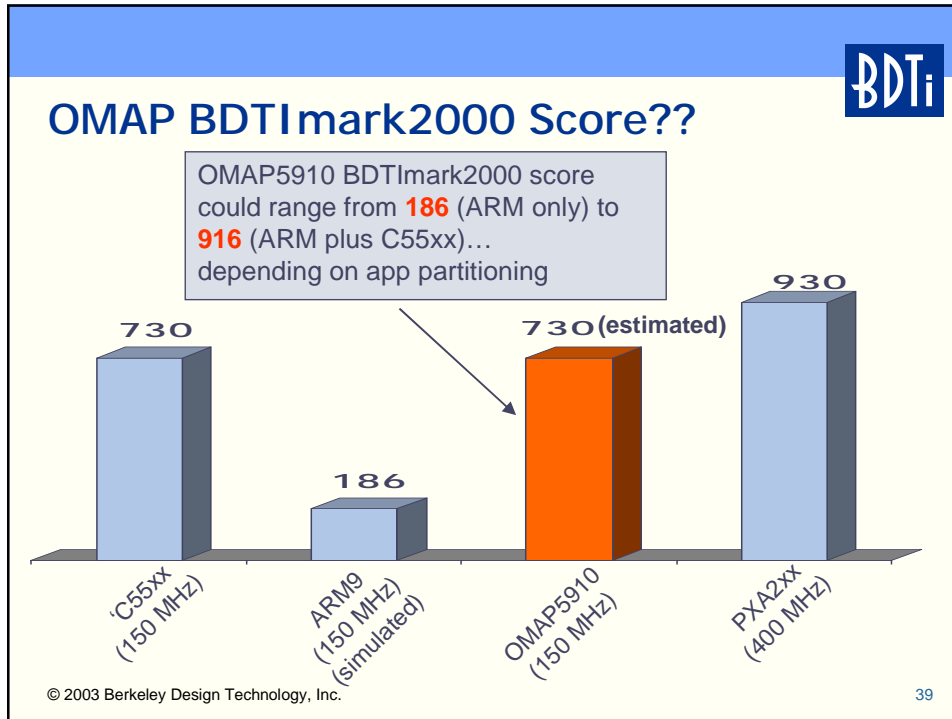


Sacrifices:

- 'C55xx not very compilable
- Dual-core approach complicates system development

© 2003 Berkeley Design Technology, Inc. 38

DSP Benchmark Results for the Latest Processors



Emerging Benchmarking Challenges

New technologies create benchmarking challenges


- Multi-core devices
- DSP-enhanced FPGAs
- Application-specific processors
- Customizable processors
- Reconfigurable processors

Evolving applications and tools also lead to new challenges

- Increasing reliance on C compilers


© 2003 Berkeley Design Technology, Inc. 40

© 2003 Berkeley Design Technology, Inc.




Application Benchmarking

- For technologies not well served by kernel benchmarks
 - DSP-enhanced FPGAs
 - Application-specific processors
- Limited applicability
- Practicality concerns can be partly addressed by
 - Using off-the-shelf implementations where available, or
 - Using simplified applications
 - E.g., BDTI's OFDM Benchmark—simplified telecom receiver



```
graph LR; In(( )) --> IQ[IQ]; IQ --> FIR[FIR Filter]; FIR --> FFT[FFT]; FFT --> Slicer[Slicer]; Slicer --> Viterbi[Viterbi]; Viterbi --> Out(( ))
```


© 2003 Berkeley Design Technology, Inc. 41



Compiler Benchmarking

- Better compilers, more compilable architectures encourage migration to C for DSP
- Processor selection may hinge on compiler quality
- But it is difficult to assess how efficient a compiler is for DSP...
 - Or to compare two compilers for the same processor
- Compiler benchmarking sounds simple, but raises complex questions...
 - Benchmark the compiler or the compiler+processor?
 - Allow intrinsics?
 - Allow C source code optimizations?
 - Allow limited assembly tweaking?
 - Where to draw the line?


© 2003 Berkeley Design Technology, Inc. 42



Conclusions

- Today's DSP-oriented processors cannot be meaningfully compared using simplified metrics
 - Relevant, meaningful benchmark results are essential to processor evaluation
- There is no ideal processor
 - Fastest doesn't mean best
 - The "best" processor depends on the details of the application
 - Different architectural approaches make different performance trade-offs
 - Understanding these is key to selecting a processor

© 2003 Berkeley Design Technology, Inc. 43




Conclusions

- Consider all the options
 - Increasing performance overlap between dissimilar architectures
 - Alternatives increasingly viable
- Application requirements and processor performance are both moving targets
- Emerging architectures and technologies require benchmarking evolution
- Factors other than performance are often important
 - Compatibility, tools, off-the-shelf software, ...

© 2003 Berkeley Design Technology, Inc. 44

DSP Benchmark Results for the Latest Processors



For More Information...

www.BDTI.com

Free Information

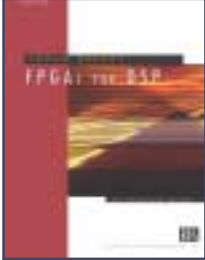
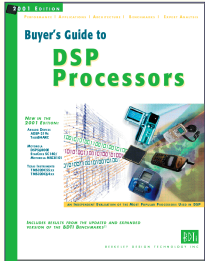
- BDTImark2000™ scores
- *DSP Insider* newsletter
- *Pocket Guide to Processors for DSP*

White papers on processor architectures and benchmarking

Article reprints on DSP-oriented processors and applications

- *EE Times*
- *IEEE Spectrum*
- *IEEE Computer* and others

comp.dsp FAQ



2001 Edition 45

© 2003 Berkeley Design Technology, Inc.