Alternatives to DSP Processors for Communications Applications

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Presentation Goals

- Why consider alternatives?
- What types of alternatives are relevant?
- Which companies are developing these?
- What are the major distinguishing characteristics of each type of alternative?
About BDTI
Independent DSP Analysis • Optimized DSP Software

- Analytical consulting services
- Publications on DSP technology
  - Buyer's Guide to DSP Processors
  - Inside the StarCore SC140
  - DSP Processor Fundamentals
- Training
- Software development services
  - Streaming media applications focus

Comms Apps: Two Types

- Infrastructure
  - Wired
    - E.g., xDSL, “cable”, VoIP gateway
  - Wireless
    - E.g., cellular, PCS, fixed wireless, satellite

- Terminals
  - Portable
    - Battery-powered, size-constrained
  - Non-portable (e.g., “CPE”)

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### Infrastructure Processor Requirements

**Key criteria**
- Performance/board area
- Performance/W
- Price/performance
- Large-system integration support
- Tools
- Application-development infrastructure
- Architecture roadmap

### Terminal Processor Requirements

**Key criteria**
- Energy efficiency
- Sufficient performance
- Cost
- Memory use
- Small-system integration support
- Tools
- Application-development infrastructure
- Packaging
- Chip-product roadmap
Why Consider Alternatives?

- **Processing throughput**
  - 3G wireless computation needs outstripping DSP processor advances
  - DSP processor performance gains coming at increased cost
- **Development**
  - DSP processor software development tools have significant weaknesses
- **Cost**
  - Desire for increased integration drives SoC adoption
- **Energy efficiency**

“As the industry shifts from second-generation, 2G, to 3G wireless we see the percentage of the physical layer MIPS that reside in the DSP dropping from essentially 100 percent in today’s technology for GSM to about 10 percent for wideband code-division multiple access (WCDMA).”

Texas Instruments
IEEE Communications Magazine
January 2000
Alternatives to DSP Processors for Communications Applications

**Processor DSP Speed:**

BDTImarks™ (Higher is Better)

<table>
<thead>
<tr>
<th>Gen</th>
<th>Year</th>
<th>Processor</th>
<th>Speed</th>
</tr>
</thead>
<tbody>
<tr>
<td>1st</td>
<td>1982</td>
<td>TMS32010</td>
<td>5 MHz</td>
</tr>
<tr>
<td>2nd</td>
<td>1987</td>
<td>DSP5601</td>
<td>13 MHz</td>
</tr>
<tr>
<td>3rd</td>
<td>1995</td>
<td>TMS320C54x</td>
<td>50 MHz</td>
</tr>
<tr>
<td>4th</td>
<td>2000</td>
<td>TMS320C6203</td>
<td>300 MHz</td>
</tr>
</tbody>
</table>

“3G” Wireless

**Energy-Flexibility Tradeoff**

Energy Efficiency vs. MOPS/mW vs. Runtime Algorithmic Flexibility

- **HW ASIC**
- **FPGA**
- **DSPs**
- **Embedded Processors**
- **Flex. Heterogeneous Multiprocessing**

Source: J. Rabaey, UCB
Key Alternatives

- General-purpose processors
- Massively parallel processors
- ASICs
- DSP, CPU, coprocessor cores
- Virtual ICs
- ASSPs
- Customizable processor cores
- Reconfigurable hardware
  - FPGAs
  - Reconfigurable processors

GPPs and Hybrids

Today, many general-purpose processors have strong DSP capabilities

- High-performance GPPs with DSP enhancements
  - E.g., Pentium III, PowerPC 7xxx
- Embedded GPPs with and without DSP enhancements
  - E.g., SH3-DSP, LX5280
  - E.g., StrongARM
GPPs and Hybrids
Strengths and Weaknesses

+ DSP performance often strong
- Often weak on integration*
+ General-purpose tools, infrastructure strong
- DSP-oriented tools, infrastructure may be weak
+ Widely known, large installed base
+ Compatibility (in some cases)
- Dynamic features can complicate real-time operation (mostly in high-perf. GPPs)

ASICs

- A chip designed for a specific end product or group of end products
- Typically contains some non-programmable hardware
  - E.g., special-purpose algorithm engines
- May contain one or more processor cores
- May be a “system on chip” with memory, peripherals, special I/O, etc.
- May use a mix of custom and licensed blocks
VLSI Technology’s GSM SoC

Source: VLSI Technology

ASICS
Strengths and Weaknesses

↑ Offers the ultimate in tailored hardware
  ↑ Speed, energy efficiency, cost/performance, ...
  ↑ Integration to match the product requirements

↓ Large development costs and risks vs. off-the-shelf hardware
  ↓ Iteration is costly and time consuming

↓ Lengthy development cycles

↓ Hardware/software integration and whole-chip testing are particularly challenging

↓ Hardware/software partitioning typically must be done early
**ASICS**

“Virtual ICs”: An Alternative Approach

An integrated behavioral model that is realizable via a variety of target architectures, platforms, and fabrication processes

![Diagram of Virtual IC and System Software](source: Ellipsis Digital Systems)

Key: Behavior decoupled from implementation

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**Customizable Cores**

- Intended for use in SoC designs
- Certain features selectable by the chip designer (e.g., a 2nd MAC unit, cache)
- Data path can be modified
- Other features may be customizable as well
- Synthesizable HDL description generated
- Software tools automatically customized
- Examples:
  - ARC, Tensilica, Improv, Carmel2000
Example Application Profile: AC-3 Audio Decoder

- IDCT: 39%
- Window: 25%
- Denorm: 11%
- Other: 25%

% time spent in each module

Tensilica Xtensa

- Base processor
- Library of standard peripherals
- Library of instr. set extensions
- Custom instr. set extensions
- Xtensa µP generator
- ALU
- IO
- Cache
- Register File
- MMU
- Tailored µP core, HDL form
- Customized compiler, assembler, linker, debugger, simulator
- Fabricate using any ASIC foundry
Customizable Cores
Strengths and Weaknesses

- DSP application characteristics mean that customization can yield huge gains
  - Speed, energy efficiency, cost/performance, ...
- Requires a very large investment
  - Must design own chip
- Tools immature
  - Additional layer of complexity in tools
- Unproven technology
- Uncertain company/technology roadmaps

Reconfigurable Processors

- Blend FPGA and processor technology
- Multiple flavors:
  - Processor core + FPGA
  - Processor core w/reconfigurable data path
  - Reconfigurable, application-specific processor (or core)

Heterogeneous, Reconfigurable Dataflow Processor

Source: MorphICs Technology, Inc.
Reconfigurable Processors
Strengths and Weaknesses

↑ DSP application characteristics mean that customization can yield huge gains
   ↑ Speed, energy efficiency, cost/performance, ...

↑ Flexibility
   ♦ Support multiple standards w/same gates
   ♦ Support field upgrades to highly specialized hardware

↓ Cost, energy have been prohibitive for high-volume and portable applications
   ↓ But application-specific approaches show promise

↓ Unproven

↓ Tools for complex DSP applications immature

Conclusions

● Options are expanding for DSP system designers
   ■ New approaches
   ■ New products
   ■ New providers

● There is no single “best” choice
   ■ Heterogeneous SoCs increasingly common

● A key challenge: Balancing architecture-specificity with generality, flexibility

● Tools, methods, verification are key
   ■ Behavior, system, software, and hardware
Resources

- www.BDTI.com
  - *DSP Insider* (free email newsletter)
  - *Pocket Guide to DSP Processors*
  - BDTImark2000™ DSP benchmark scores
  - White papers, article reprints

Employment Opportunities

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  - Near San Francisco and U.C. Berkeley
  - Away from the crowds of Silicon Valley
- Excellent working environment
  - Interesting, varied projects
  - The latest DSP technology and applications
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