Speed per Square Milimeter Ratios for Fixed-Point Licensable Cores (65 nm)

Updated October 2009

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See page 3 for details.

All processors benchmarked with 16-bit fixed-point data. All cores include at least 16 KB on-core memory and use worst-case clock speeds for the TSMC CLN65GP process and the Artisan Advantage core cell library. Vendors can choose different speed/area/power trade-offs; to understand the trade-offs, please view all BDTI metrics for each core. BDTIsimMark2000™ scores may be based on projected clock speeds. For information, see www.BDTI.com/Services/Benchmarks

¹Coreworks scores include both a customized SideWorks DSP engine and the FireWorks 32-bit RISC processor. The SideWorks core used to implement the BDTI DSP Kernel Benchmarks includes four 16-bit multiplier units, six 32-bit ALUs, five shift units, six data multiplexing units, two data de-multiplexing units, two bit-reverse units, a bit unpack unit, and 6K bytes of memory. Different versions of the SideWorks core will yield different performance, power consumption, and die size figures than those reported here.
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Speed vs. Area for Fixed-Point Licensable Cores (65 nm)
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![BDTI logo]

<table>
<thead>
<tr>
<th>Processor Family</th>
<th>Clock Rate</th>
<th>BDTImark2000™, BDTIsimMark2000™</th>
<th>Die Area</th>
<th>BDTImark2000™/mm², BDTIsimMark2000™/mm²</th>
</tr>
</thead>
<tbody>
<tr>
<td>Coreworks Sideworks CWcomp4465¹</td>
<td>383</td>
<td>4470</td>
<td>0.987 mm²</td>
<td>4530</td>
</tr>
</tbody>
</table>

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**Clock rate:** Clock speeds assume worst-case process, voltage, and temperature variations

**Die area:** Die area for core only; does not include area for caches or other memories

**BDTImark2000™, BDTIsimMark2000™:** The BDTImark2000™ and BDTIsimMark2000™ provide a summary measure of signal processing speed. BDTIsimMark2000™ scores may be based on projected clock speeds. For more info and scores see www.BDTI.com/Services/Benchmarks.