

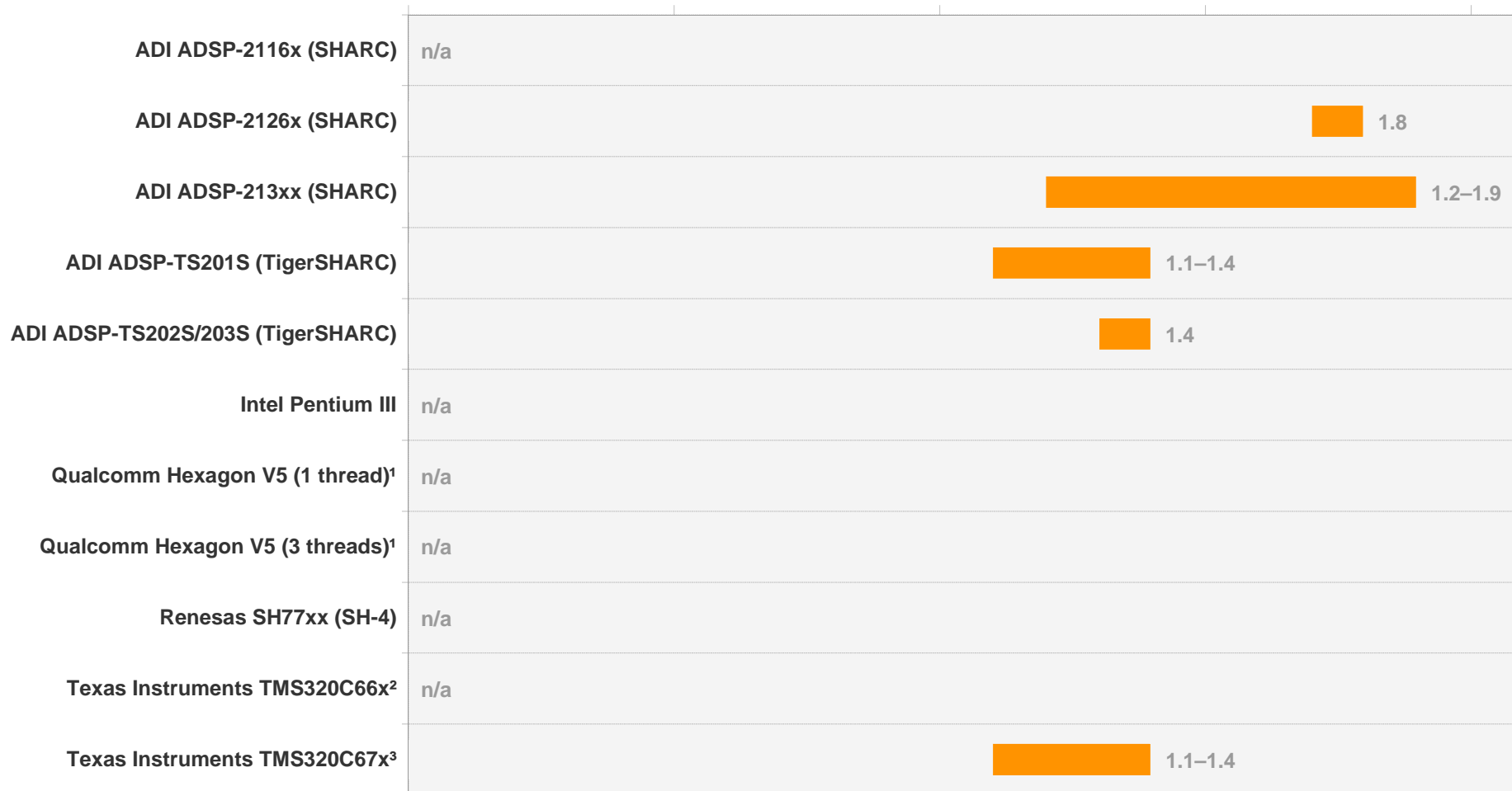
Speed per Milliwatt Ratios for Floating-Point Packaged Processors

Updated May 2013

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See page 2 for details.



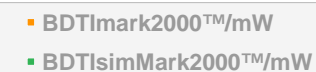
¹ Lower range of score is official single-thread BDTI^{sim}Mark2000, higher score is projected best case score using the maximum number of available threads (not an official BDTI^{sim}Mark2000 score).

² Score for one core

³ Score does not apply to TMS320C67x+ parts (e.g., the TMS320C672x)

All processors benchmarked with 32-bit floating-point data.

BDTI^{sim}Mark2000™ scores may be based on projected clock speeds. For information, see www.bdti.com/Services/Benchmarks.



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Processor Family	Clock Rate (min-max)	BDTI ^{mark} 2000™, BDTI ^{sim} Mark2000™ (min-max)	Power (min-max)	BDTI ^{mark} 2000™/mW, BDTI ^{sim} Mark2000™/mW (min-max)
ADI ADSP-2116x (SHARC)	100–110 MHz	550–600	n/a	n/a
ADI ADSP-2126x (SHARC)	150–200 MHz	820–1090	450–600 mW	1.8
ADI ADSP-213xx (SHARC)	200–400 MHz	1020–2050	n/a	1.2–1.9
ADI ADSP-TS201S (TigerSHARC)	500–600 MHz	3730–4480	2583–3907 mW	1.1–1.4
ADI ADSP-TS202S/203S (TigerSHARC)	500 MHz	3620	2583 mW	1.4
Intel Pentium III	1400 MHz	3130	n/a	n/a
Qualcomm Hexagon V5 (1 thread) ¹	100–267 MHz (per thread)	900–2400 (1 Thread)	n/a	n/a
Qualcomm Hexagon V5 (3 threads) ¹	100–267 MHz (per thread)	900–2400 (1 Thread)	n/a	n/a
Renesas SH77xx (SH-4)	333–400 MHz	1040–1250	n/a	n/a
Texas Instruments TMS320C66x ²	850–1500 MHz	7290–12860	n/a	n/a
Texas Instruments TMS320C67x ³	150–300 MHz	750–1500	533–1372 mW	1.1–1.4

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BDTI^{mark}2000™, BDTI^{sim}Mark2000™: The BDTI^{mark}2000™ and BDTI^{sim}Mark2000™ provide a summary measure of signal processing speed. BDTI^{sim}Mark2000™ scores may be based on projected clock speeds. For information see www.BDTI.com/Services/Benchmarks.

Note: In general, BDTI^{mark}2000™/mW and BDTI^{sim}Mark2000™/mW scores cannot be computed from the speed and power data presented here. For example, the fastest processors are not always the highest-power processors. Therefore, it is not always possible to calculate a speed per milliwatt ratio by dividing the maximum speed for a family by the maximum power for the family.