

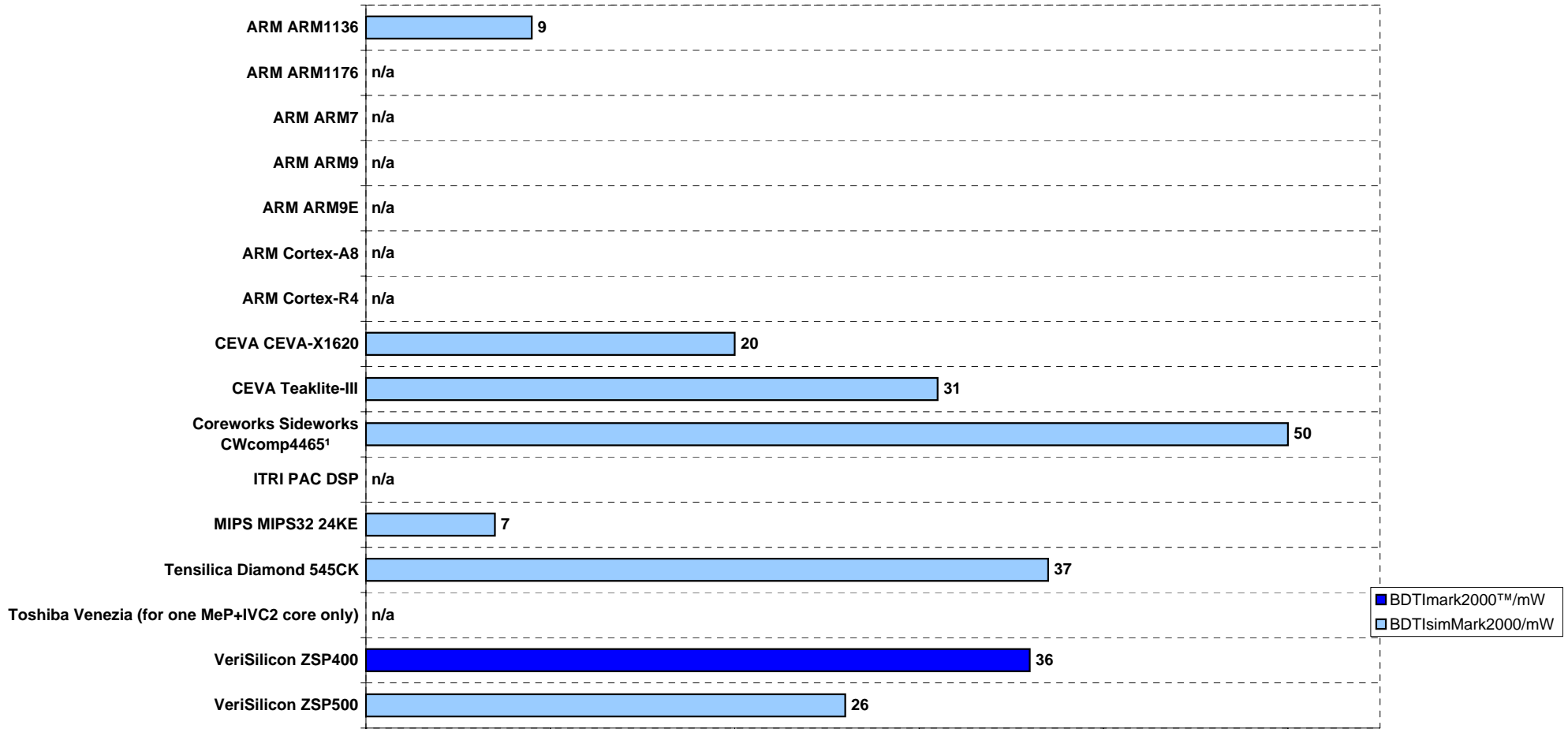
Speed per Milliwatt Ratios for Fixed-Point Licensable Cores

Updated June 2009

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See page 3 for details.



All processors benchmarked with 16-bit fixed-point data. All scores use worst-case clock speeds for the TSMC CL013G process and ARM Artisan SAGE-X library. Vendors can choose different speed/area/power trade-offs; to understand the trade-offs, please view all BDTI metrics for each core. BDTIsimMark2000™ scores may be based on projected clock speeds. For information, see www.BDTI.com/benchmarks.html.
¹Coreworks scores include both a customized SideWorks DSP engine and the FireWorks 32-bit RISC processor. The SideWorks core used to implement the BDTI DSP Kernel Benchmarks includes four 16-bit multiplier units, six 32-bit ALUs, five shift units, six data multiplexing units, two data de-multiplexing units, two bit-reverse units, a bit unpack unit, and 6K bytes of memory. Different versions of the SideWorks core will yield different performance, power consumption, and die size figures than those reported here.

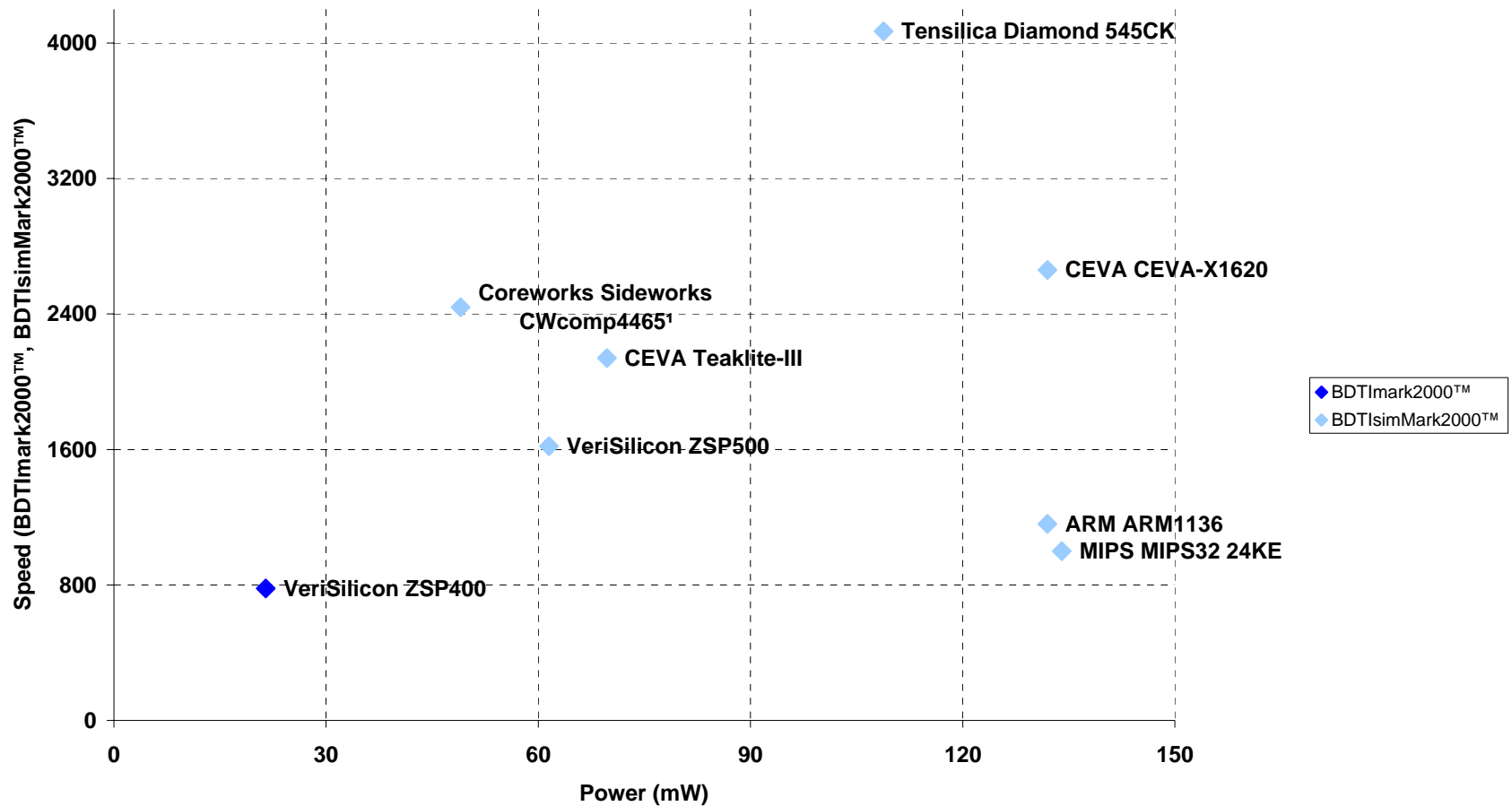
Speed vs. Power for Fixed-Point Licensable Cores

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| Processor Family | Clock Rate | BDTImark2000™, BDTIsimMark2000™ | Power | BDTImark2000™/mW, BDTIsimMark2000™/mW |
|--|------------|------------------------------------|--------|--|
| ARM ARM1136 | 330 | 1160 | 132 mW | 9 |
| ARM ARM1176 | 335 | 1200 | n/a | n/a |
| ARM ARM7 | 145 | 160 | n/a | n/a |
| ARM ARM9 | 255 | 320 | n/a | n/a |
| ARM ARM9E | 265 | 550 | n/a | n/a |
| ARM Cortex-A8 | n/a | n/a | n/a | n/a |
| ARM Cortex-R4 | n/a | n/a | n/a | n/a |
| CEVA CEVA-X1620 | 330 | 2660 | 132 mW | 20 |
| CEVA Teaklite-III | 335 | 2140 | 70 mW | 31 |
| Coreworks Sideworks CWcomp4465 ¹ | 209 | 2440 | 49 mW | 50 |
| ITRI PAC DSP | n/a | n/a | n/a | n/a |
| MIPS MIPS32 24KE | 335 | 1000 | 134 mW | 7 |
| Tensilica Diamond 545CK | 245 | 4070 | 109 mW | 37 |
| Toshiba Venezia (for one MeP+IVC2 core only) | n/a | n/a | n/a | n/a |
| VeriSilicon ZSP400 | 165 | 780 | 21 mW | 36 |
| VeriSilicon ZSP500 | 205 | 1620 | 62 mW | 26 |

All processors benchmarked with 16-bit fixed-point data. All results assume use of the TSMC CL013G process and the ARM Artisan SAGE-X library. Vendors can choose different speed/area/power trade-offs; to understand the trade-offs, please view all BDTI metrics for each core.

¹Coreworks scores include both a customized SideWorks DSP engine and the FireWorks 32-bit RISC processor. The SideWorks core used to implement the BDTI DSP Kernel Benchmarks includes four 16-bit multiplier units, six 32-bit ALUs, five shift units, six data multiplexing units, two data de-multiplexing units, two bit-reverse units, a bit unpack unit, and 6K bytes of memory. Different versions of the SideWorks core will yield different performance, power consumption, and die size figures than those reported here.

Clock rate: Clock speeds assume worst-case process, voltage, and temperature variations

Power: Power estimates assume typical process, voltage, and temperature variations

Power for core only; does not include power for caches or other memories

BDTImark2000™, BDTIsimMark2000™: The BDTImark2000™ and BDTIsimMark2000™ provide a summary measure of signal processing speed. BDTIsimMark2000™ scores may be based on projected clock speeds.

For more info and scores see www.BDTI.com/benchmarks.html