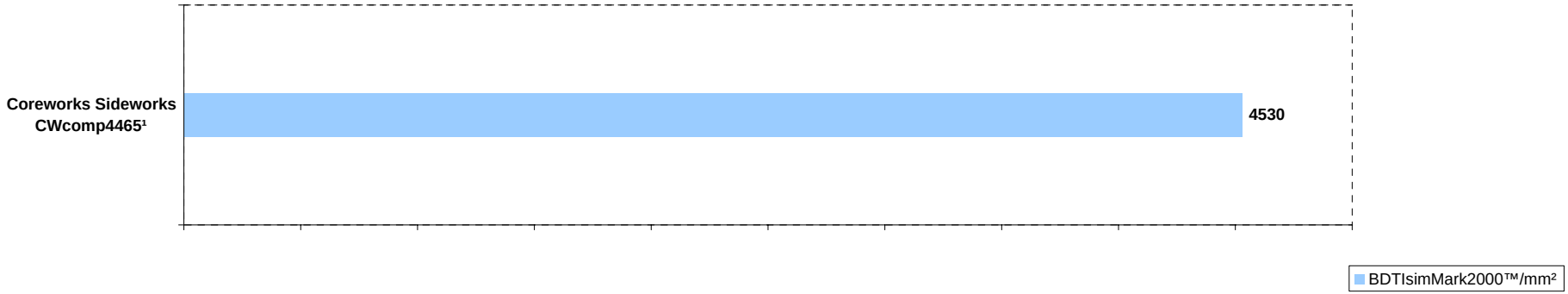
Speed per Square Milimeter Ratios for Fixed-Point Licensable Cores (65 nm)

Updated October 2009

Contact BDTI for authorization to publish scores.

See page 3 for details.



All processors benchmarked with 16-bit fixed-point data. All cores include at least 16 KB on-core memory and use worst-case clock speeds for theTSMC CLN65GP process and the Artisan Advantage core cell library. Vendors can choose different speed/area/power trade-offs; to understand the trade-offs, please view all BDTI metrics for each core. BDTIsimMark2000™ scores may be based on projected clock speeds. For information, see www.BDTI.com/benchmarks.html.

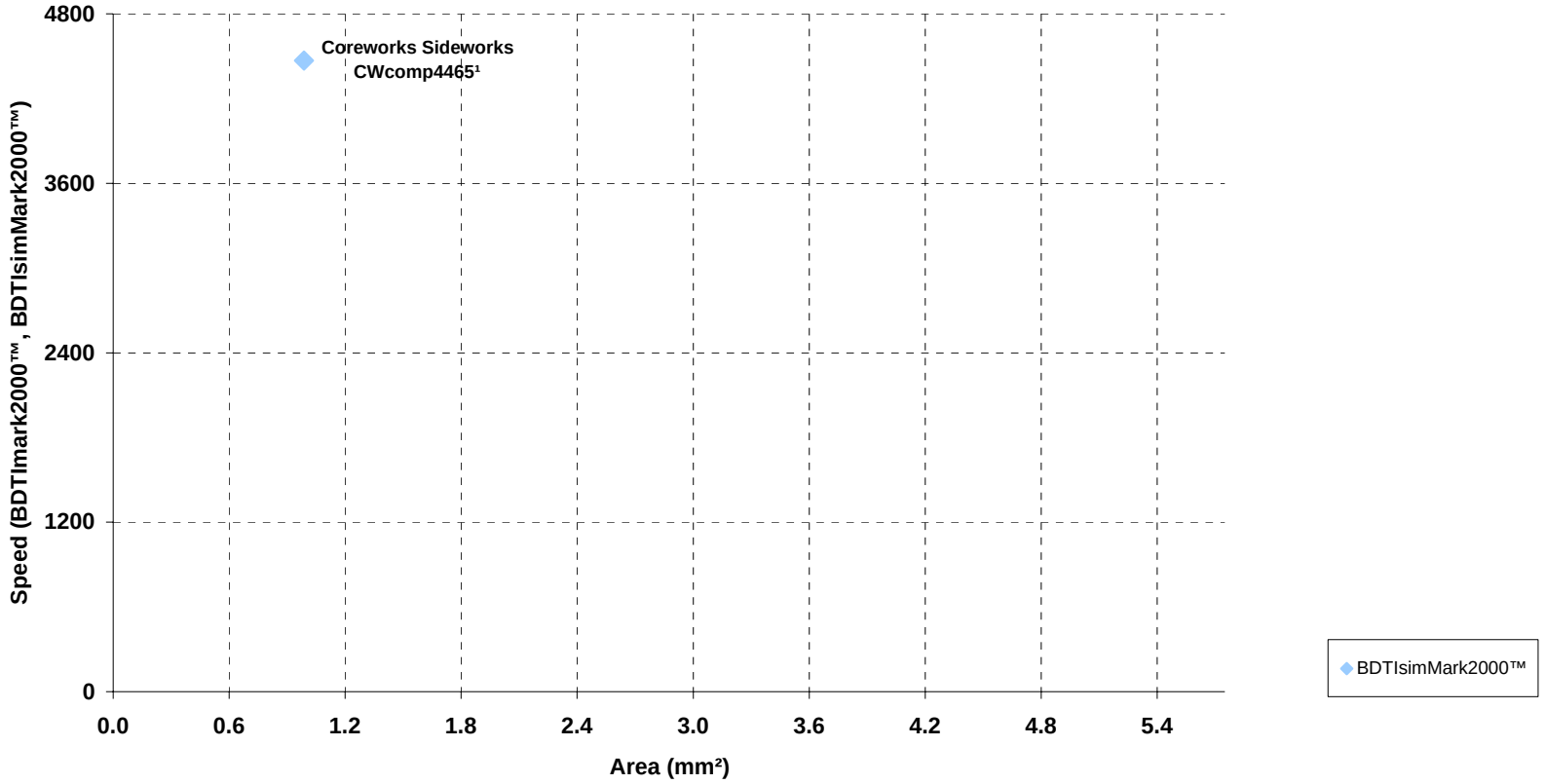
[1]Coreworks scores include both a customized SideWorks DSP engine and the FireWorks 32-bit RISC processor. The SideWorks core used to implement the BDTI DSP Kernel Benchmarks includes four 16-bit multiplier units, six 32-bit ALUs, five shift units, six data multiplexing units, two data de-multiplexing units, two bit-reverse units, a bit unpack unit, and 6K bytes of memory. Different versions of the SideWorks core will yield different performance, power consumption, and die size figures than those reported here.

Speed vs. Area for Fixed-Point Licensable Cores (65 nm)

Updated October 2009

Contact BDTI for authorization to publish scores.

See page 3 for details.



All processors benchmarked with 16-bit fixed-point data. All cores include at least 16 KB on-core memory and use worst-case clock speeds for theTSMC CLN65GP process and the Artisan Advantage core cell library. Vendors can choose different speed/area/power trade-offs; to understand the trade-offs, please view all BDTI metrics for each core. BDTIsimMark2000™ scores may be based on projected clock speeds. For information, see www.BDTI.com/benchmarks.html.

¹Coreworks scores include both a customized SideWorks DSP engine and the FireWorks 32-bit RISC processor. The SideWorks core used to implement the BDTI DSP Kernel Benchmarks includes four 16-bit multiplier units, six 32-bit ALUs, five shift units, six data multiplexing units, two data de-multiplexing units, two bit-reverse units, a bit unpack unit, and 6K bytes of memory. Different versions of the SideWorks core will yield different performance, power consumption, and die size figures than those reported here.

Speed vs. Area for Fixed-Point Licensable Cores (65 nm)

Updated October 2009

Processor Family	Clock Rate	**BDTImark2000™**, *BDTIsimMark2000™*	Die Area	**BDTImark2000™/mm²**, *BDTIsimMark2000™/mm²*
Coreworks Sideworks CWcomp4465[1]	383	*4470*	0.987 mm²	*4530*

All processors benchmarked with 16-bit fixed-point data. All cores include at least 16 KB on-core memory and use worst-case clock speeds for theTSMC CLN65GP process and the Artisan Advantage core cell library. Vendors can choose different speed/area/power trade-offs; to understand the trade-offs, please view all BDTI metrics for each core. BDTIsimMark2000™ scores may be based on projected clock speeds. For information, see www.BDTI.com/benchmarks.html.

[1]Coreworks scores include both a customized SideWorks DSP engine and the FireWorks 32-bit RISC processor. The SideWorks core used to implement the BDTI DSP Kernel Benchmarks includes four 16-bit multiplier units, six 32-bit ALUs, five shift units, six data multiplexing units, two data de-multiplexing units, two bit-reverse units, a bit unpack unit, and 6K bytes of memory. Different versions of the SideWorks core will yield different performance, power consumption, and die size figures than those reported here.

Clock rate: Clock speeds assume worst-case process, voltage, and temperature variations
Die area: Die area for core only; does not include area for caches or other memories
BDTImark2000™, BDTIsimMark2000™: The BDTImark2000™ and BDTIsimMark2000™ provide a summary measure of signal processing speed. BDTIsimMark2000™ scores may be based on projected clock speeds.
For more info and scores see www.BDTI.com/benchmarks.html