Independent DSP Benchmarking: Methodologies and Latest Results

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Outline

- Motivation for benchmarking
- DSP benchmarking approaches--pros and cons
- Benchmark performance of example processors
- The BDTImark: what is it?
- Factors influencing benchmark results
- General-purpose processors for DSP
- Conclusions

Motivation for Benchmarking

- Need quick and accurate comparisons of processors' DSP performance
- As architectures diversify, it becomes more difficult to compare performance
- There is a need for independent processor evaluations

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DSP Benchmarking Approaches

There are a number of DSP benchmarking approaches. The main candidates are:

- Simplified metrics (MIPS, MOPS, etc)
- Complete DSP applications
- DSP algorithm "kernels"

What's Wrong with MIPS?

Why not rely on MIPS, MOPS, MACs/sec, MFLOPS...?

These metrics are simple and easy to measure, but can be misleading. Questions to ponder:

- Just what is an "instruction" or "operation"? (or, when is 100 MIPS faster than 120 MIPS?)
- What's included in a MAC, and what if my application does something besides MACs?

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Benchmarking Full Applications

Why not just use a full DSP application, like a V.34 modem or GSM cell phone?

This approach has a number of problems:

- Applications tend to be ill-defined
- Costly, time-consuming to implement
- Evaluates programmer as much as processor
- Measures *system*, not just processor

What's an Algorithm Kernel?

An algorithm kernel forms the heart of an algorithm.

Algorithms, in turn, form the heart of a DSP application.

Example algorithm kernels include FFTs, IIR filters, convolutional encoders, etc.

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Why Use Algorithm Kernels?

Algorithm kernels are good benchmark candidates because they are:

- Relevant
- Practical to specify and implement
- Relatively simple to optimize

BDTI Benchmarking Methodology

- Benchmarks are rigorously defined
- All implementations follow the same rules
- Benchmarks are hand-optimized in assembly
- Each benchmark is independently verified for performance, functionality, optimality, conformance to benchmark specs
- Benchmarks use processor's native data format

BDTI Benchmarking Methodology

- Benchmarks optimized for speed, then memory usage (except FSM, which is the other way around)
- BDTI's benchmarks reveal realistic performance, not necessarily fastest possible performance
- Benchmarks are architecture-independent; can be implemented on any processor (including general-purpose processors)

BDTI Benchmark™ Suite

Composed of 11 DSP algorithm kernels.

On each benchmark, we measure five quantities:

- Cycle count
- Execution time
- Cost-performance
- Energy Consumption
- Memory use

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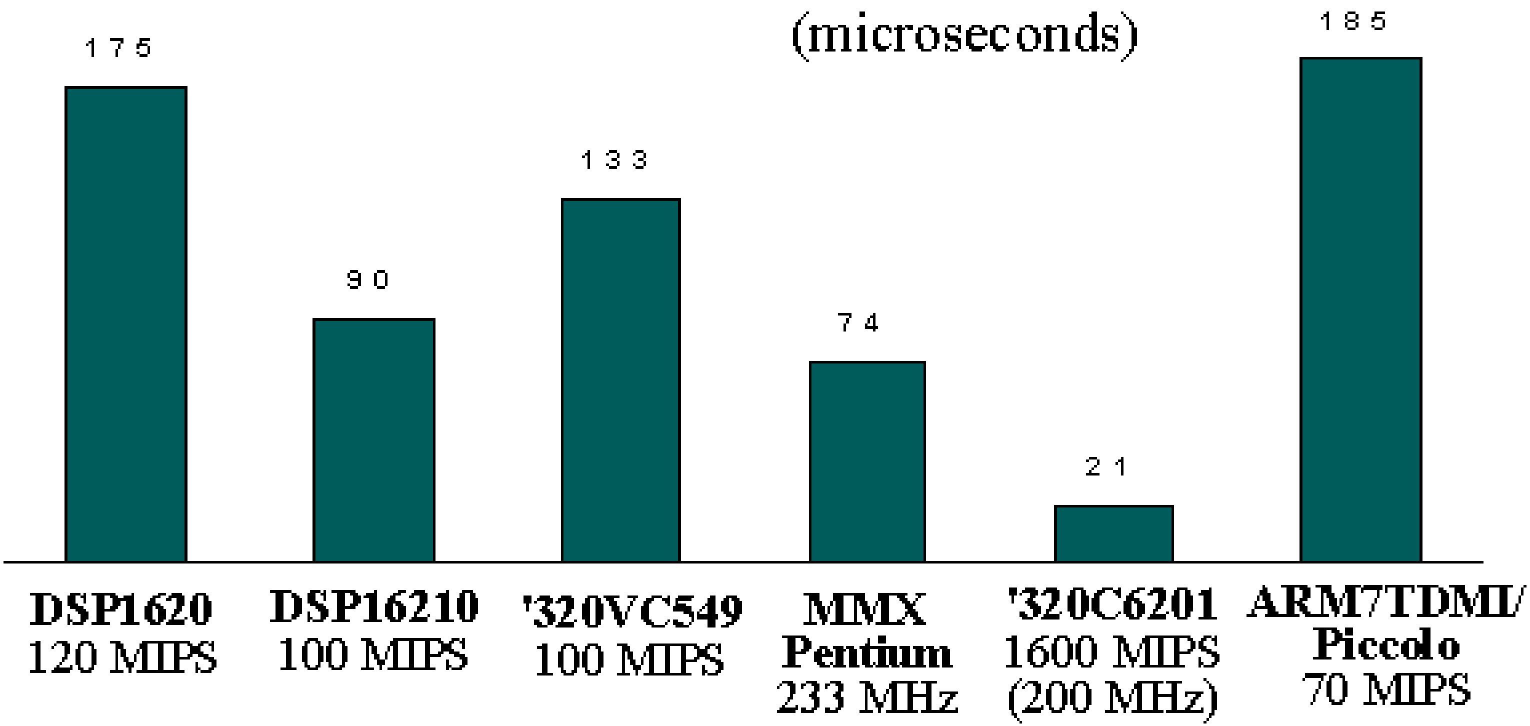
Execution Times: FFT Benchmark*



*All benchmark results in this presentation are taken from BDTI's reports, *Buyer's Guide to DSP Processors, 1999 Edition, DSP on General-Purpose Processors*, and *Inside the ARM Piccolo*

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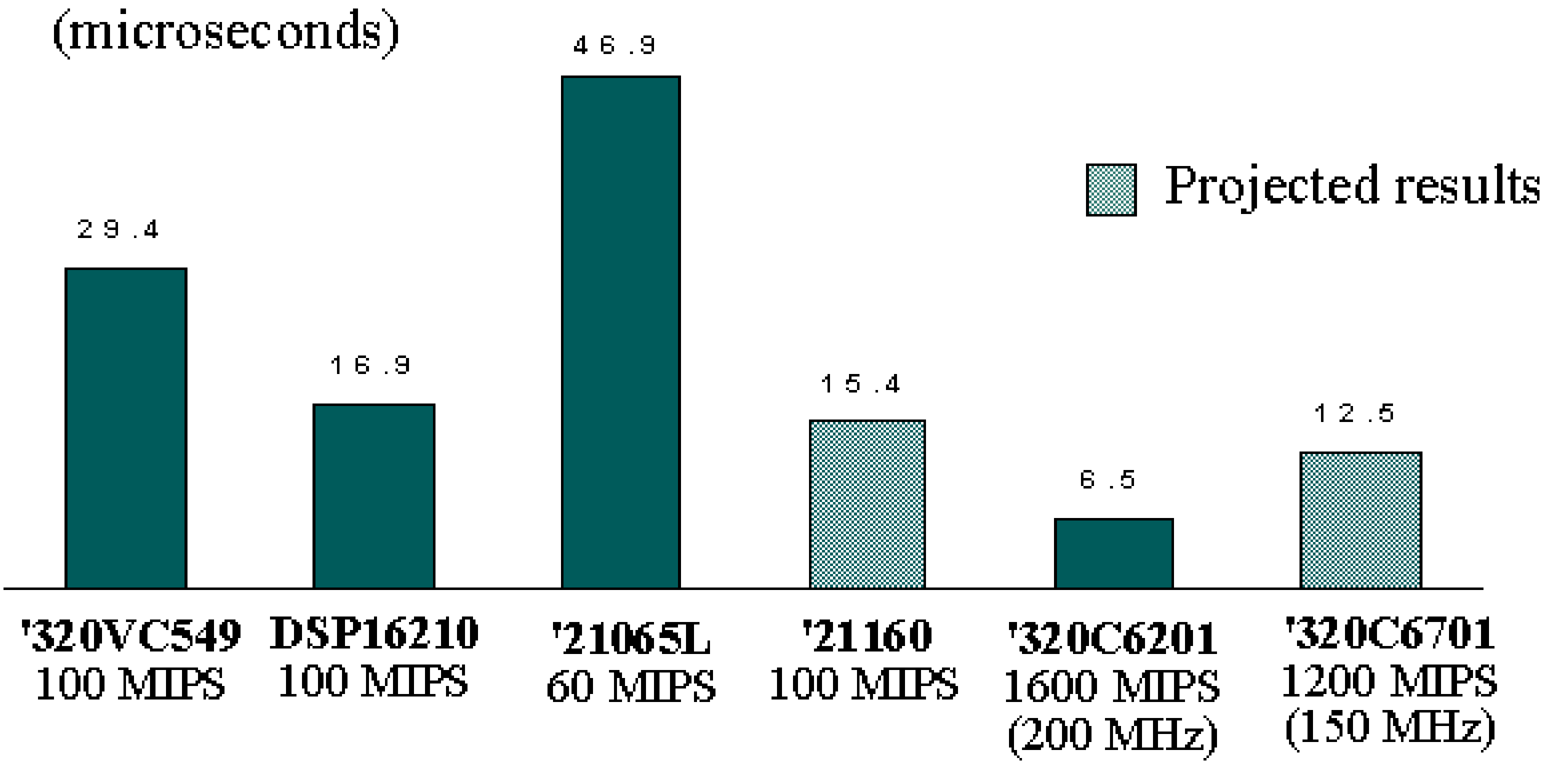
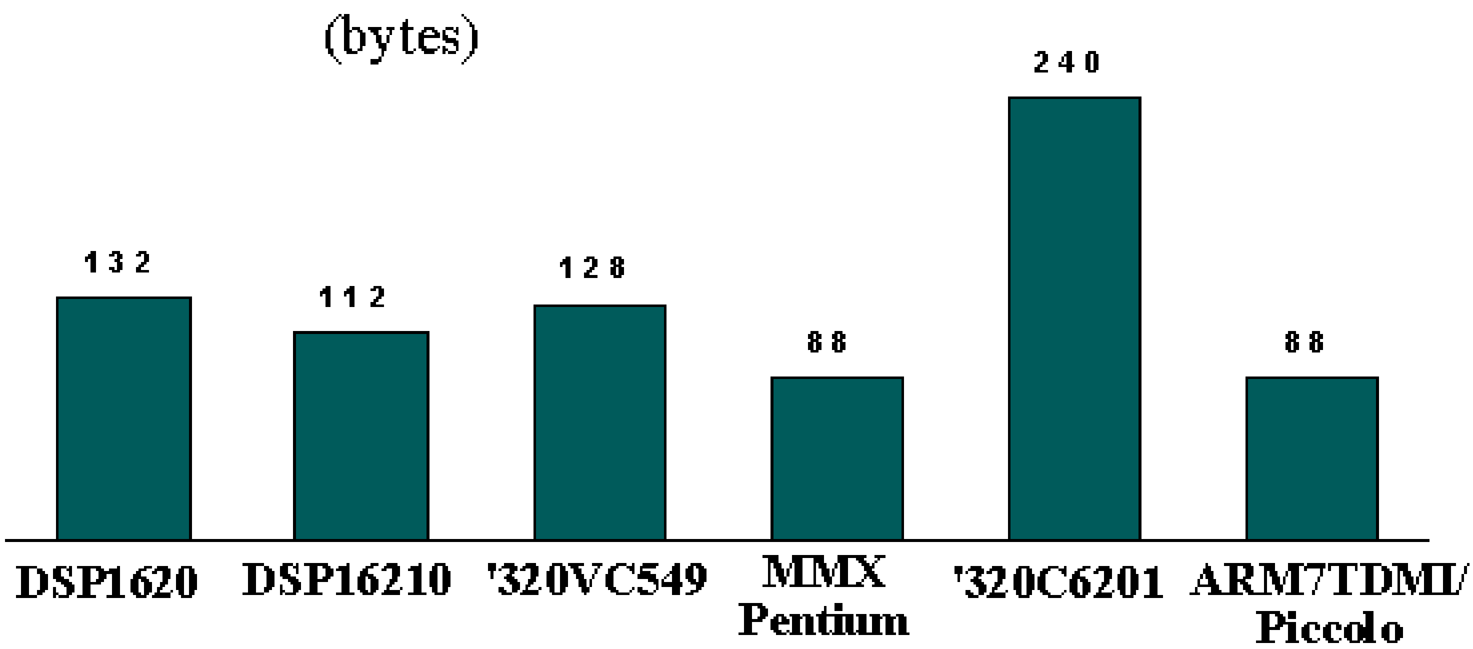
Execution Times: Complex Block FIR

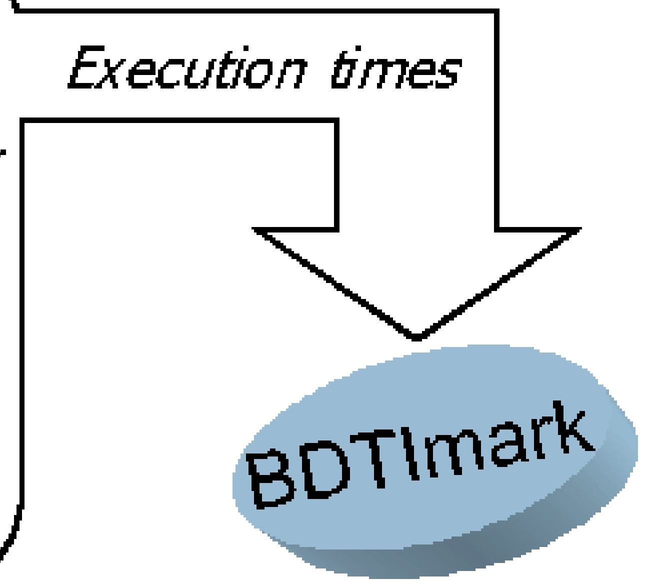


Memory Usage: FSM Benchmark

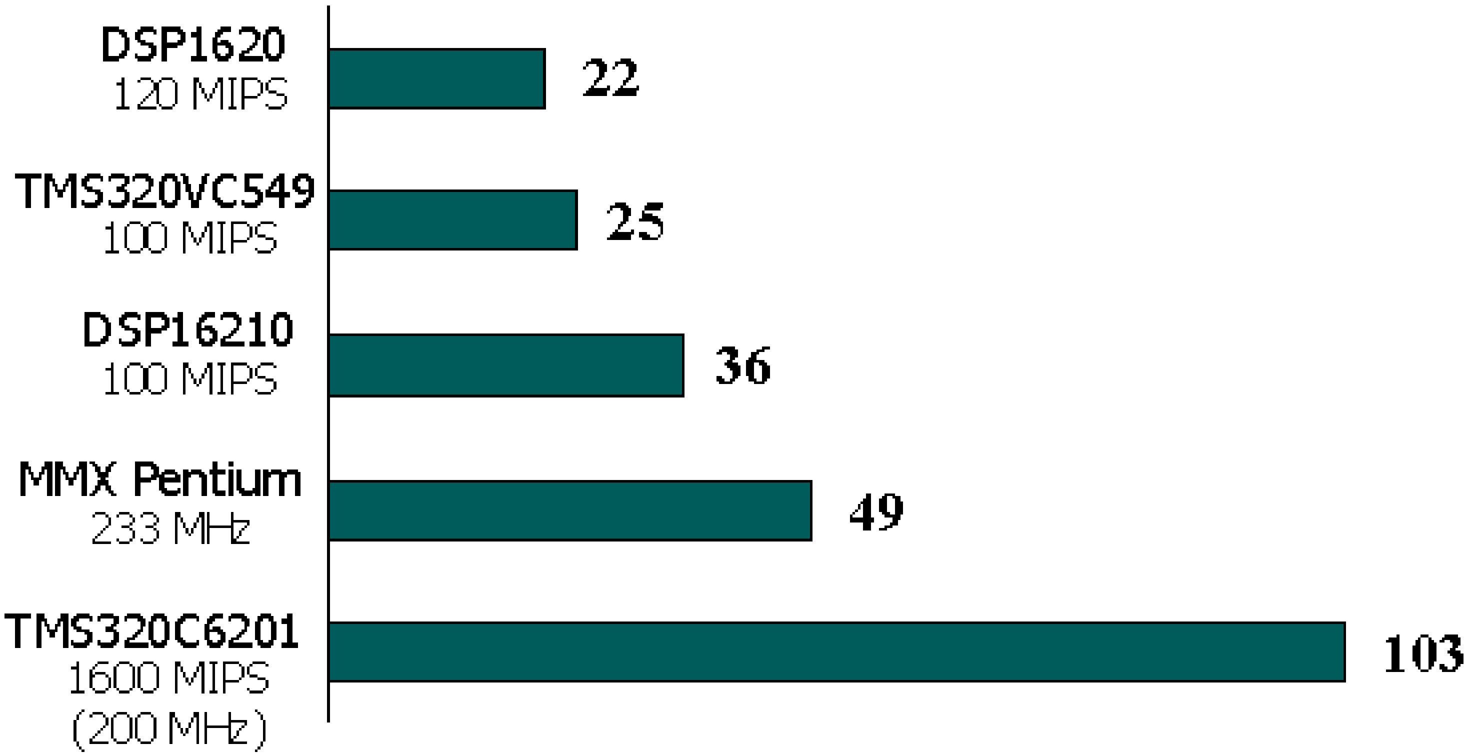


The BDTImark™

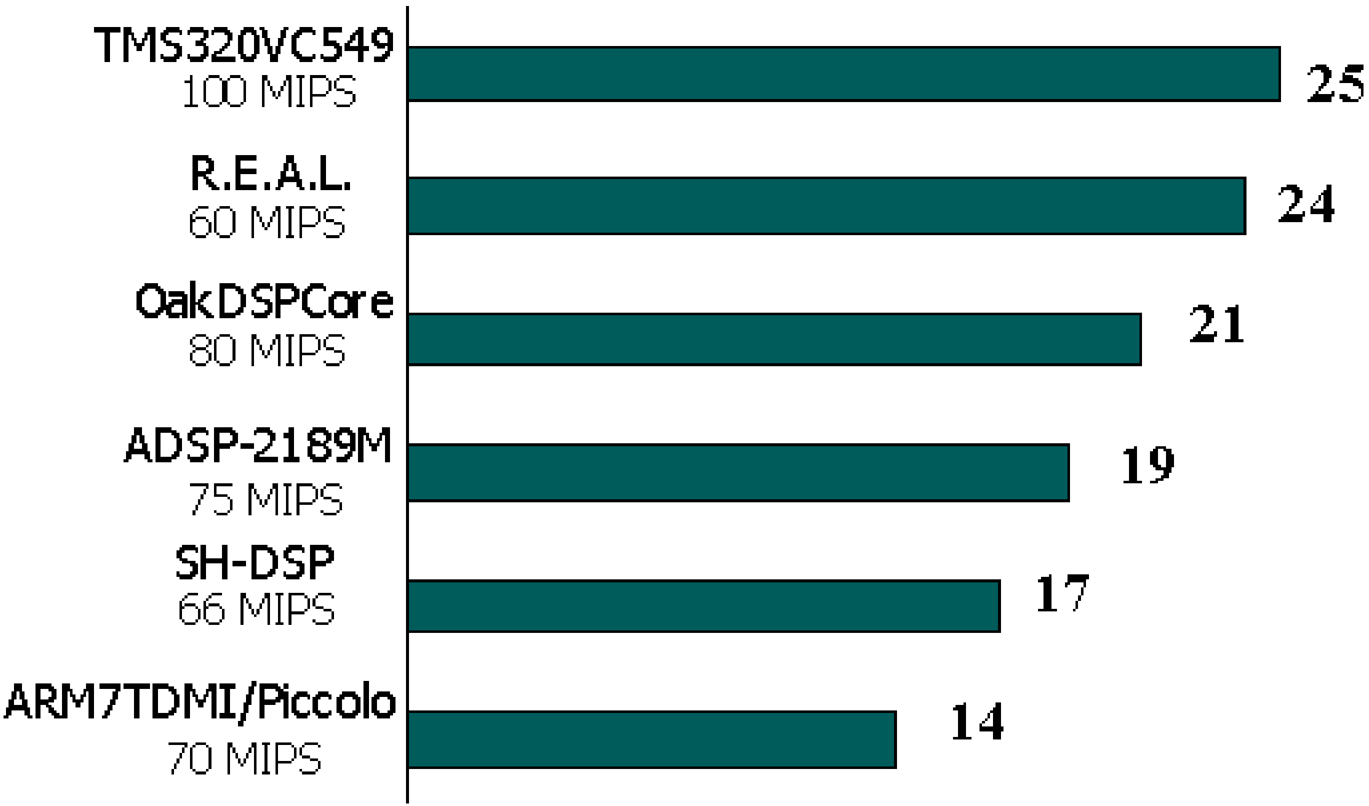
- Real block FIR filter
- Complex block FIR filter
- Single-sample real FIR filter
- Single-sample LMS-adaptive FIR filter
- Single-sample IIR filter
- Vector dot product
- Vector add
- Vector maximum
- IS-54 convolutional encoder
- Finite state machine
- 256-point FFT



Example BDTImark Results



Example BDTImark Results



What Factors Influence Benchmark Results?

Factors

- Parallel execution units
- VLIW
- Superscalar
- SIMD capabilities
- Instruction-word size
- RISC-like instructions vs complex, compound instructions
- Memory bandwidth
- Pipeline
- Hardware accelerators

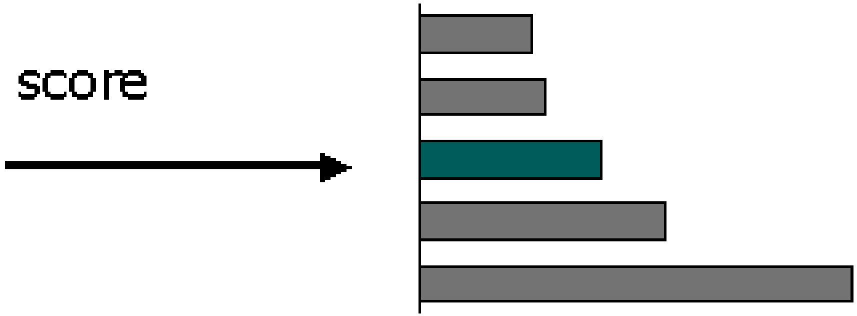
- Clock speed

Case Study: The DSP16xxx

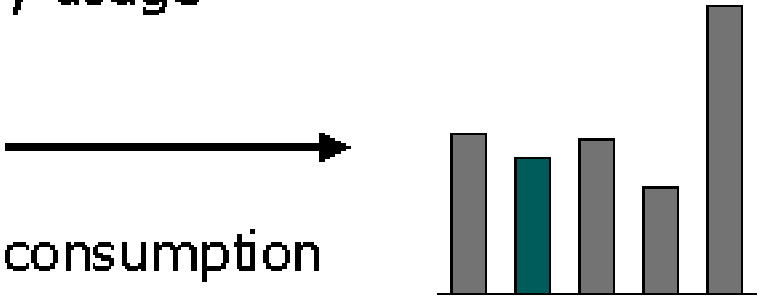
- Traditional DSP architecture, but with major additions
- Dual multipliers, wider memory buses yield 2 MACs/cycle
- Complex instructions, restrictions on parallel operations and register usage
- Simple pipeline

The DSP16210

- Good BDTImark score



- Moderate memory usage



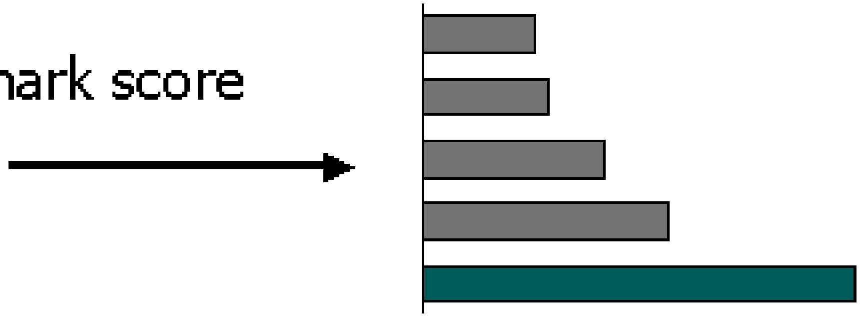
- Moderate power consumption

Case Study: The TMS320C62xx

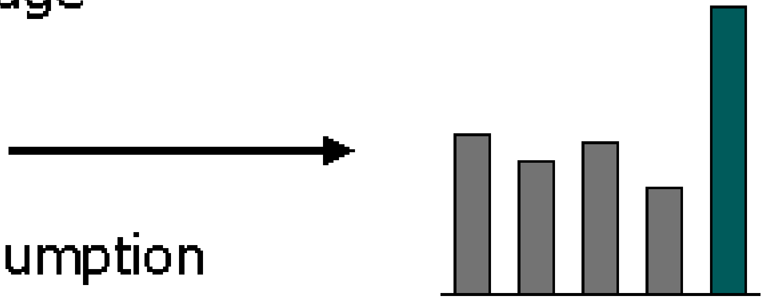
- Radical new VLIW-like architecture
- Simple, RISC-like instructions with few restrictions
- 8 execution units (including 2 multipliers and 4 ALUs) produce 2 MACs/cycle
- Deep, complicated pipeline

The TMS320C6201

- Excellent BDTImark score



- High memory usage



- High power consumption

GPPs for DSP

High-End GPPs for DSP

Today's high-end general-purpose processors outperform many DSPs *even on DSP applications.* Why?

- Blazing clock speeds
- Superscalar execution
- Branch prediction, speculative execution
- Integrated DSP-oriented features

Drawbacks of High-End GPPs

Even when their performance is competitive, high-end GPPs don't usually replace DSPs because of:

- Unpredictable execution times
- Poor cost-performance relative to fixed-point DSPs
- High power consumption
- A lack of DSP-oriented development tools

If a high-end GPP is already present in the system, it may be attractive to use it for DSP work. Otherwise, it's often better to use a DSP.

Embedded GPPs for DSP

- GPPs for embedded applications are starting to address DSP needs
  - Hitachi SH-DSP, ARM Piccolo, Siemens TriCore
- These processors achieve reasonable DSP performance while maintaining relatively low cost & low power consumption
- Embedded GPPs typically don't have the advanced features that affect execution time predictability, so are easier to use for DSP

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Conclusions

- Rigorous benchmark specs are essential
- The "best" processor depends on the application
- The fastest processor for a DSP task may not be a DSP
- Metrics other than execution speed may be most important
- Benchmarks don't tell the whole story

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For More Information...

Free resources on BDTI's web site,

http://www.bdti.com

- *Evaluating DSP Processor Performance,* a white paper from BDTI
- *DSP Processors Hit the Mainstream* reprinted from IEEE Computer Magazine
- Numerous other BDTI article reprints, slides
- *comp.dsp* FAQ
- BDTImark scores