Optimized DSP Software • Independent DSP Analysis

Evaluating FPGAs For Communication Infrastructure Applications

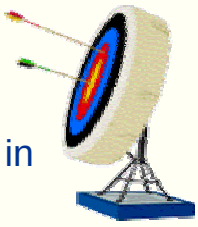
Berkeley Design Technology, Inc.
2107 Dwight Way, Second Floor
Berkeley, California 94704
USA
+1 (510) 665-1600

info@BDTI.com
http://www.BDTI.com

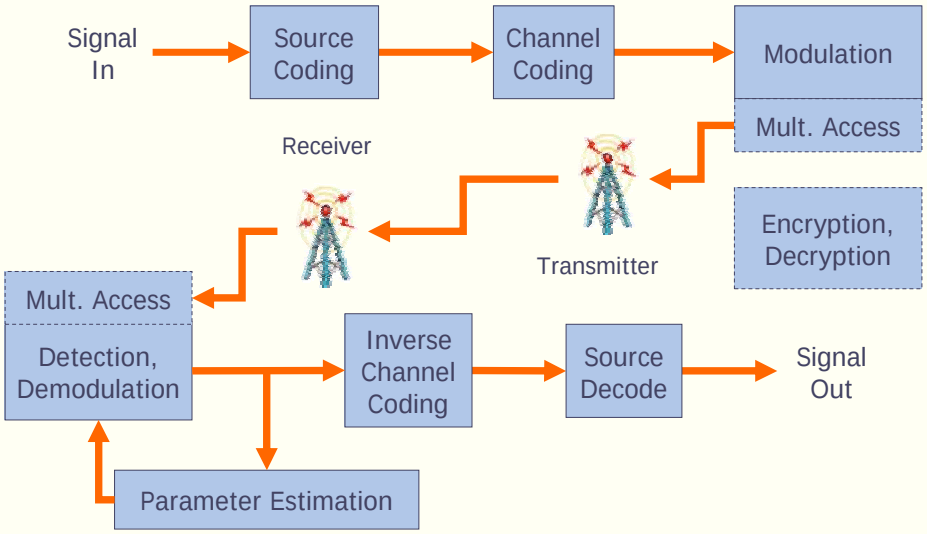
Presentation Goals

By the end of this workshop, you should know:

- Key processor-selection criteria and trends for communication infrastructure
- Key strengths and weaknesses of high-end DSPs
- Key strengths and weaknesses of high-end FPGAs
- How typical DSPs and FPGAs stack up in terms of performance and cost/perf.



Generalized Comm System



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Systems: Two Types

Infrastructure
- Examples: base stations, central office equipment, cable "head-end"

Terminals
- Portable
  - Battery-powered, size-constrained
  - Examples: cellular phone, mobile media player, PDA
- Non-portable (e.g., "CPE")
  - Examples: set-top box, home media server

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Terminal Requirements

Key criteria

- Sufficient performance
- Cost
- Energy efficiency
- Memory use
- Small-system integration support
- Packaging
- Tools
- Application-development infrastructure
- Chip-product roadmap

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Infrastructure Requirements

Key criteria

- Board area per channel
- Power per channel
- Cost per channel
- Large-system integration support
- Tools
- Application-development infrastructure
- Architecture roadmap
  - Compatibility, multi-vendor support

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Key Processing Technologies

DSPs

GPPs/DSP-enhanced GPPs

Reconfigurable architectures
- **FPGAs**
- Reconfigurable processors

Massively parallel processors

ASSPs

ASICs
- Licensable cores
- Customizable cores
- Platform-based design

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DSPs: The Incumbents

Modern conventional DSPs introduced ~1986
- One instruction, one MAC per cycle
- Developed primarily for telecom applications

High-performance VLIW DSPs introduced ~1997
- Developed primarily for wireless infrastructure
- Speed focused:
  - Independent execution units support many instructions, MACs per cycle
  - Deeper pipelines and simpler instruction sets support higher clock rates
- Emphasis on compilability

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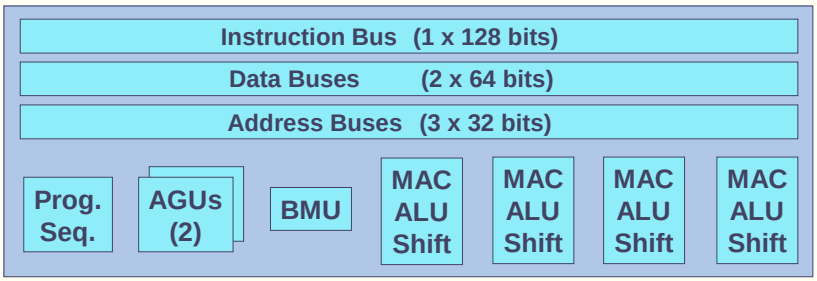
Example: StarCore SC140

Motorola, Agere,... and now Infineon

- 6-issue 16-bit fixed-point architecture
  - Up to four 16-bit MACs per cycle
- Motorola MSC8101 (one SC140 core) shipping at 300 MHz, $116 (1 ku)



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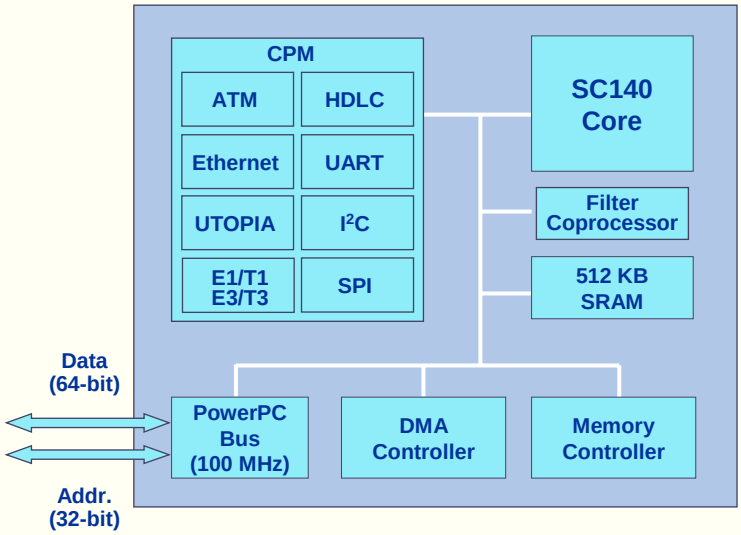
Motorola MSC8101



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Other Infrastructure DSPs

Texas Instruments TMS320C64x
- 8-issue 16-bit fixed-point architecture
  - Up to four 16-bit MACs per cycle
  - Special instructions and co-processors for communications
  - Compatible with 'C62x, 'C67x
- Sampling at 720 MHz, $216 (1 ku)
  - Shipping at 600 MHz, $108 (1 ku)

Analog Devices TigerSHARC (ADSP-TS20x)
- 4-issue fixed- and floating-point
  - Up to eight 16-bit fixed-point MACs per cycle
  - Special instructions for 3G base stations
  - High memory bandwidth (18 GB/s)
- Sampling at 600 MHz, $334 (1 ku)
  - TS101 shipping at 300 MHz, $234 (1 ku)

DSP Processors

Strengths and Weaknesses

- DSP performance, efficiency strong compared with other types of off-the-shelf processors
- But may not be adequate for demanding tasks
  - Fixed architectures limit efficiency, design flexibility
  - Centralized computation and extensive indirection reduce efficiency
- Relatively limited selection of chips per family
- But products offer strong, relevant integration

DSP Processors

Strengths and Weaknesses

- Relatively low development cost, risk
  - Mature technology
  - Large, experienced developer base
  - Fast time-to-market
  - Some architectures available from multiple vendors

    But some vendors' roadmaps are unclear or uncertain

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Why Consider Alternatives?

Convergence
- DSP-intensive products increasingly include complex non-DSP functionality

Processing throughput, density
- E.g., 3G wireless computation demands outstripping DSP processor advances

Development
- DSP processor software development tools (e.g., compilers) have significant limitations

Cost
- Desire for integration drives SoC approach

Energy efficiency

Flexibility

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Wireless Bandwidth Growth

2G	2.5G	3G
• GSM	• GPRS	• 3GPP-DS-FDD
• DSC1800	• HCSD	• 3GPP-DS-TDD
• PCS1900	• IS-95C	• 3GPP-MC
• IS-95B	• IS-136+	• ARIB W-CDMA
• IS-54B	• IS-136 HS	• IS-2000 CDMA
• IS-136	• Compact EDGE	• IS-95-HDR
• PDC		

8-13 Kbps **64-384 Kbps** **384-2000+ Kbps**

NARROWBAND CIRCUIT VOICE → **WIDEBAND PACKET DATA**

~100 MIPS → **~10,000 MIPS** → **~100,000 MIPS**

Source: MorphICs Technology, Inc.

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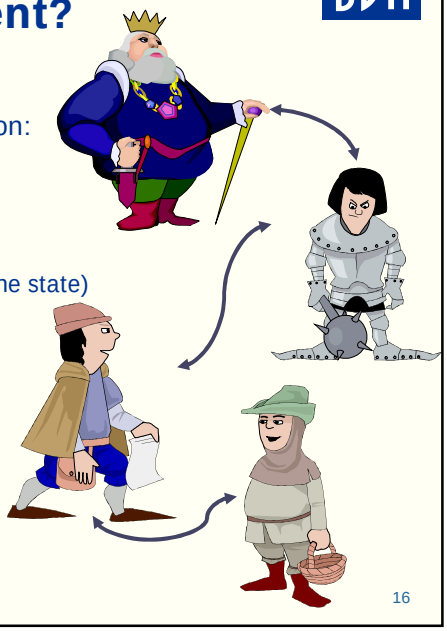
Are Processors Efficient?

The Monarchial Model of Computing

Steps for performing one basic operation:

- Fetch instruction from memory
- Decode instruction
- Compute address
- Fetch data
  - (Off-chip memory → L2, update cache state)
  - (L2 → L1, update cache state)
  - L1 → registers
  - Registers → arithmetic unit
- **Perform desired operation**
- Write result
  - Compute address, access hierarchy
- Update data pointers
- Update program counter



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FPGAs

Field-Programmable Gate Arrays

An amorphous "sea" of reconfigurable logic with reconfigurable interconnect
- Possibly interspersed with fixed-logic resources, e.g., processors, multipliers

Potential for very high parallelism

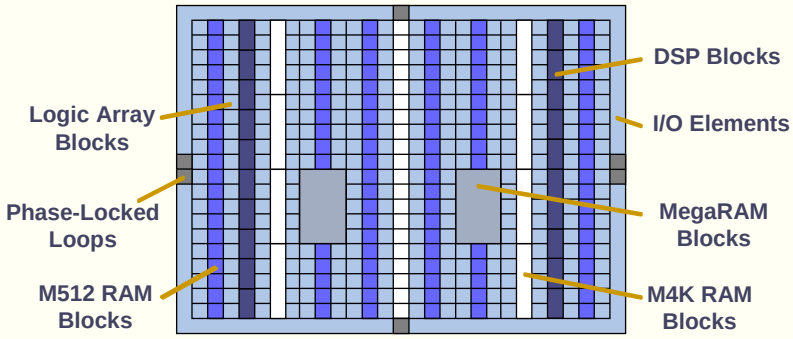
Historically used for prototyping and "glue logic," but becoming more sophisticated
- DSP-oriented architecture features
- DSP-oriented tools and design libraries
  - Viterbi, Turbo, and Reed-Solomon coders and decoders, FIR filters, FFTs,...

Key DSP players: Altera and Xilinx

Altera Stratix

Up to 28 hard-wired "DSP blocks"
- 8×9-bit, 4×18-bit, 1×36-bit multiply operations
- Optional pipelining, accumulation, etc.

Three sizes of hard-wired memory blocks



Altera Stratix

High-end, DSP-enhanced FPGAs

IP blocks
- Filters, FFTs, Viterbi decoders,...
- Nios processor
- Third-party IP, e.g., DMA controllers

DSP tools
- Parameterized IP block generators
- Simulink to FPGA link
- C+Simulink to FPGA design flow

Most family members available now

Prices begin at $170 (1 ku)

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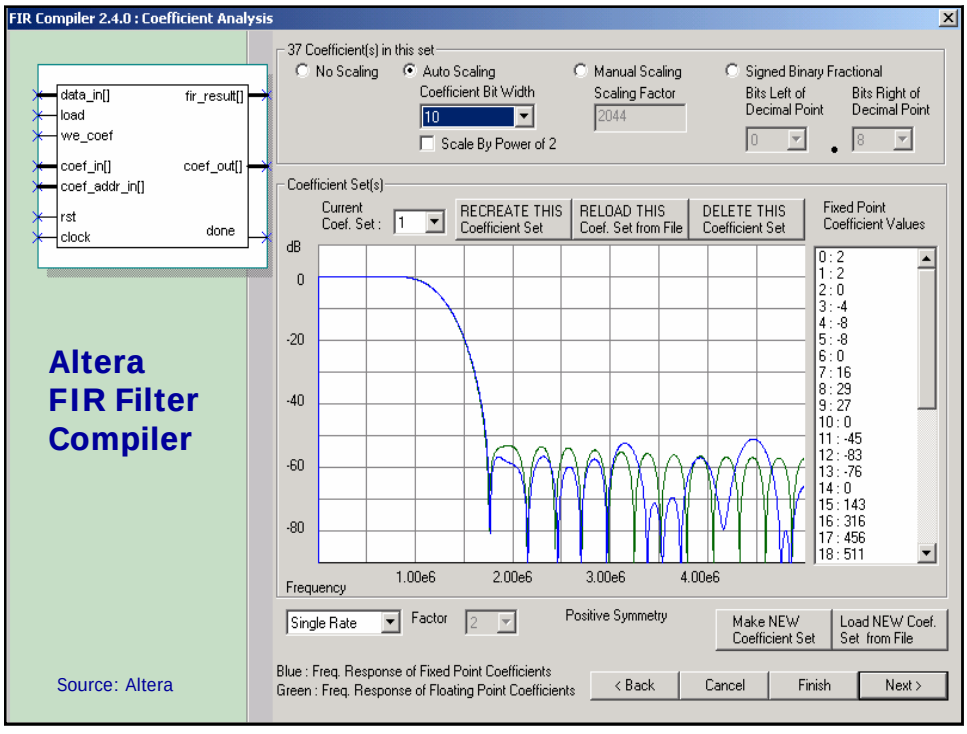


Xilinx

"Virtex" line of FPGAs

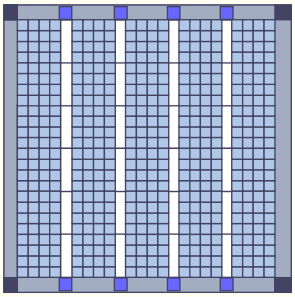
Virtex-II

- Includes array of hard-wired 18 × 18 multipliers plus distributed memory
- Up to 168 multipliers in biggest chip
- Most versions shipping now

Virtex-II Pro: joint effort with IBM

- Adds up to four hard-wired PowerPC 405 cores
- Up to 216 multipliers in biggest chip
- Most versions shipping now

Prices begin at $169 (1 ku)



Source: Xilinx

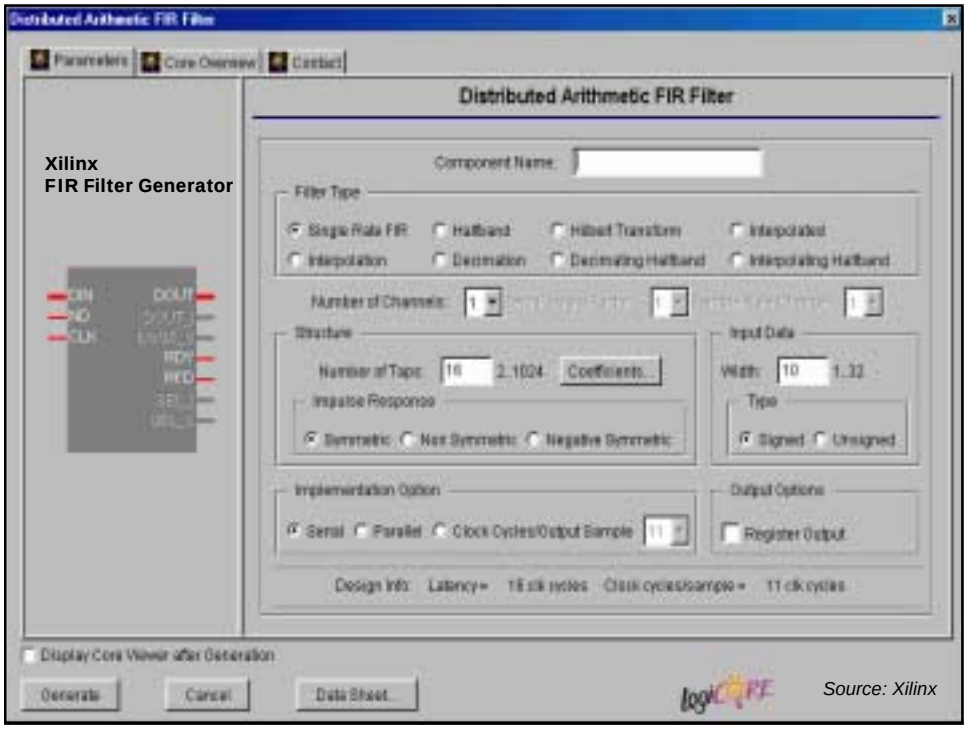
Xilinx

Soft IP blocks; e.g.,

- Reed-Solomon encoder, Viterbi decoder, turbo decoder
- ARC processor, MicroBlaze CPU

Sophisticated "Core Generator" tool for generating parameterized IP blocks

Simulink to FPGA link via "System Generator"



Source: Xilinx

Performance Analysis

- Comparing performance of off-the-shelf DSPs to that of FPGAs is tricky
- The common MMACS metric is oversimplified to the point of absurdity
  - FPGA vendors use distributed-arithmetic benchmarks that require fixed coefficients
  - MMACS metric overlooks need to dedicate resources to non-MAC tasks
  - MMACS metric ignores memory bandwidth needed to feed MACs
  - Many important DSP algorithms don't use MACs at all!

Alternative Approach: Application Benchmarks

Use a full application, e.g., N channels of an OFDM receiver

Hazards:

- Applications tend to be ill-defined
- Hand-optimization usually required in real-world applications
  - Costly, time-consuming to implement
  - Evaluates programmer as much as processor
  - What is a "reasonable" benchmark implementation?

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Solution: Simplified Application Benchmark

BDTI's benchmark is based on a simplified OFDM receiver

- Closely resembles a real-world application
- Simplified to enable optimized implementations
- Constrained to ensure consistent, reasonable implementation practices

Benchmark implementer goals:

- Maximize number of channels
- Minimize cost per channel

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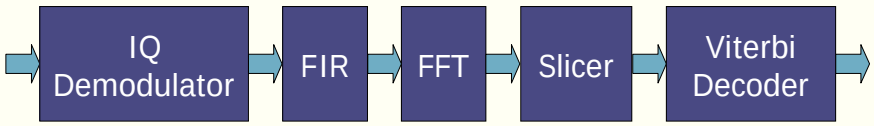
Benchmark Overview

Flexibility is an asset:

- Algorithms range from table look-ups to MAC-intensive transform
- Data sizes range from 4 to 16 bits
- Data rates range from 40 to 320 MB/s
- Data includes real and complex values



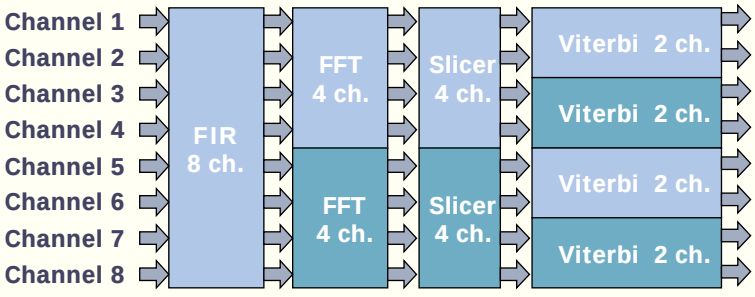
Benchmark Requirements

"Pins to pins"

Real-time throughput

Bit-exact output data

Resource sharing is permitted

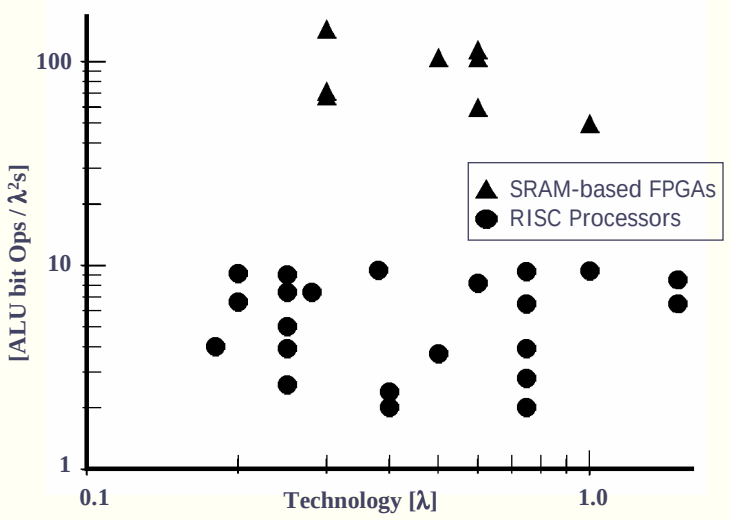


BDTI Communications Benchmark™

	Motorola MSC8101 (300 MHz)	Altera Stratix 1S20-6 (Preliminary)	Altera Stratix 1S80-6 (Preliminary)
Channels	<<1	~10	~50
Cost (1 ku)	$116	$325	$3,480

From BDTI's report, *FPGAs for DSP*.

Density Comparison



Source: Andre DeHon

FPGAs

Strengths and Weaknesses

- Massive performance gains on some algorithms
- Architectural flexibility can yield efficiency
  - Adjust data widths throughout algorithm
  - Parallelism where you need it
  - Massive on-chip memory bandwidth
- Efficiency compromised by generality
  - Embedded MAC units and memory blocks improve efficiency but reduce generality
- Potentially good cost and energy efficiency
  - But absolute prices and power consumption are much higher than DSPs'

FPGAs

Strengths and Weaknesses

- Development is long and complicated
  - Higher complexity inherent due to flexibility
  - Design flow is unfamiliar to most DSP engineers
  - But cost and complexity is much lower than ASICs'
- Development infrastructure badly lags DSPs'
  - DSP-oriented tools are immature
- Field reconfigurability (for some products)
- Reconfigure hardware for diverse tasks
- Xilinx has mature products, but others are playing catch-up

Why Use a DSP?

- Some applications are not amenable to FPGA implementations
  - Parallelism is sometimes inherently limited
  - Ultimate speed is not always the first priority
- FPGAs are still too expensive for terminal applications
- FPGA energy efficiency is still an unknown
- Implementing a complex algorithm is much more difficult on an FPGA than on a DSP

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Grading the Alternatives

	DSPs	GPPs	FPGAs	Custom Cores	ASICs	ASSPs
Design Effort	B	A	D	C	E	A+
Design Flexibility	E	E	B	C	A	E
Run-time Flexibility	C	B	A	C	E	E
Top Speed	D	E	B	C	A	A
Energy Efficiency	C	D	C	B	A	A

A = Best, E = Worst

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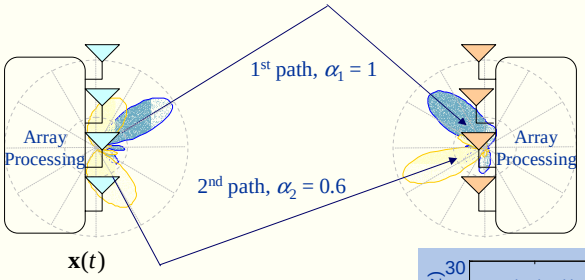
Future Communications Applications

Dealing with Non-ideal Channels

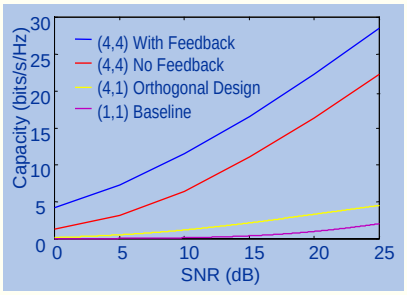


Source: Jan Rabaey, Berkeley Wireless Research Center

Multi-antenna approach exploits multi-path fading by sending data along good channels

Results in large theoretical improvements in bandwidth efficiency for fading channels

But ... computationally hungry



Conclusions

High-end FPGAs can outstrip DSPs on certain DSP tasks

- Computation-intensive, highly parallelizable tasks

High-end FPGAs are expensive, but they can beat DSPs in terms of performance per dollar

DSP have the advantage in development infrastructure, time-to-market, developer familiarity.

In many applications, a heterogeneous combination of computing engines is desirable

- Expect to see more heterogeneous processor chips

The “best” architecture depends on the details of the application

For More Information...

www.BDTI.com

Free Information

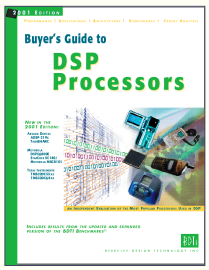
- BDTImark2000™ scores
- *DSP Insider* newsletter
- *Pocket Guide to Processors for DSP*

White papers on processor architectures and benchmarking

Article reprints on DSP-oriented processors and applications

- *EE Times*
- *IEEE Spectrum*
- *IEEE Computer* and others

comp.dsp FAQ



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