Separating Reality from Hype in Processors' DSP Performance

Berkeley Design Technology, Inc.
+1 (510) 665-1600
info@BDTI.com

www.BDTI.com

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Evaluating DSP Performance

- Essential part of processor selection
- Becoming more difficult as processor architectures diversify
- Are vendor performance claims credible?

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Approaches to Evaluating DSP Performance

Candidate approaches:

- Simplified metrics
  - E.g., MIPS (Millions of Instructions Per Second), MOPS, MMACS
- Complete DSP applications
  - E.g., v.90 modem
- DSP algorithm "kernel" benchmarks
  - E.g., FIR filter, FFT

What's Wrong with MIPS?

MIPS and MFLOPS (Millions of Floating-Point Operations per Second) are frequently used as shorthand for processor speed. But are they really meaningful?

Two instructions from different processors:

DSP16210

```
A0=A0+P0+P1 P0=Xh*Yh P1=Xl*Yl Y=*R0++ X=*PT0++
```

TMS320C6201

```
ADD   A0,A3,A0
```

Benchmarking Full Applications

Why not just use a full DSP application, like a v.90 modem or AC-3 decoder?

This approach is common in PC systems (e.g., SPEC) but is not appropriate for DSP benchmarking because:

- Applications tend to be ill-defined
- Hand-optimization in assembly language is usually required in real-world applications
  - Costly, time-consuming to implement
  - Evaluates programmer as much as processor
- Measures *system*, not just processor

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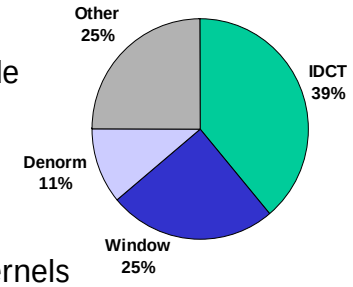
Algorithm Kernel Benchmarks

- DSP algorithm kernels are the most computationally intensive portions of DSP applications
- Example algorithm kernels include
  - FFTs
  - IIR filters
  - Viterbi decoders
- Application-relevant algorithm kernels are strong predictors of overall performance



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Vendor Benchmarks

- Many processor vendors provide DSP algorithm kernel benchmark results for their own processors, but in general
  - Benchmarks are not standardized across vendors
  - Results are not independently verified
  - Clock speeds are often projected
- These results are then often misused, for example,
  - Comparing their fastest chip to the slowest from another vendor
  - Comparing vaporware to real silicon
  - Presenting cycle counts as an indication of performance
  - Cherry-picking benchmark results

BDTI Benchmarking Methodology

- BDTI uses algorithm kernel benchmarks
  - Rigorously defined
  - Hand-optimized in assembly
  - All implementations follow the same rules
  - The most important rule is that only “realistic” optimizations are allowed
- Each benchmark is independently verified for:
  - Performance
  - Functionality
  - Optimality
  - Conformance to benchmark spec

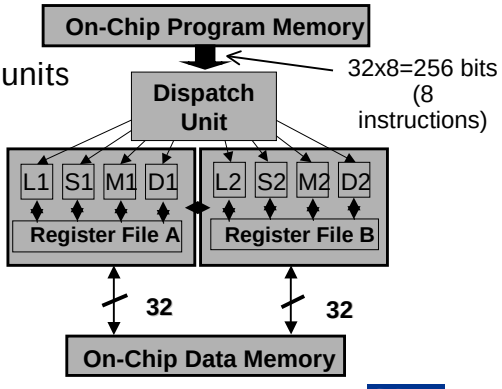
Separating Reality from Hype

We will use the BDTI Benchmarks to evaluate vendor performance claims regarding:

- Speed (execution times)
- Energy Efficiency
- Memory Use

Texas Instruments TMS320C62xx

- First commercial VLIW-based DSP
- Introduced in 1997
- 8-issue with 8 execution units
- 11-stage pipeline
- At its introduction, projected to operate at 200 MHz (1600 MIPS)



TMS320C62xx

"10x the Performance of Available DSPs"

– TI's February 1997 slideshow describing the TMS320C62xx

- Based on projected speed of 200 MHz (1600 MIPS); initial samples ran at 120 MHz

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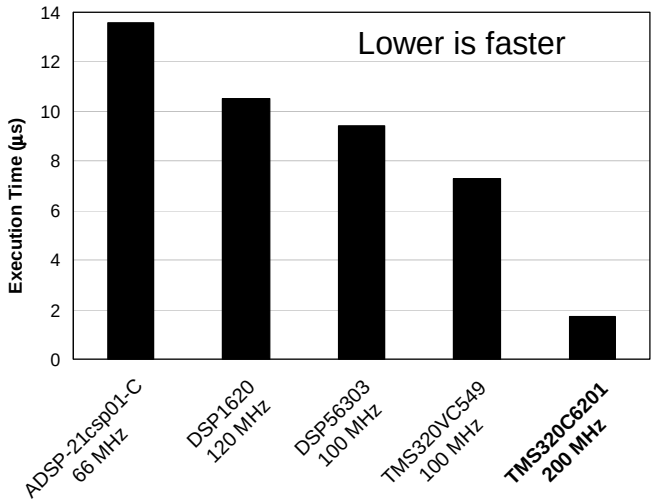
Real Block FIR Benchmark



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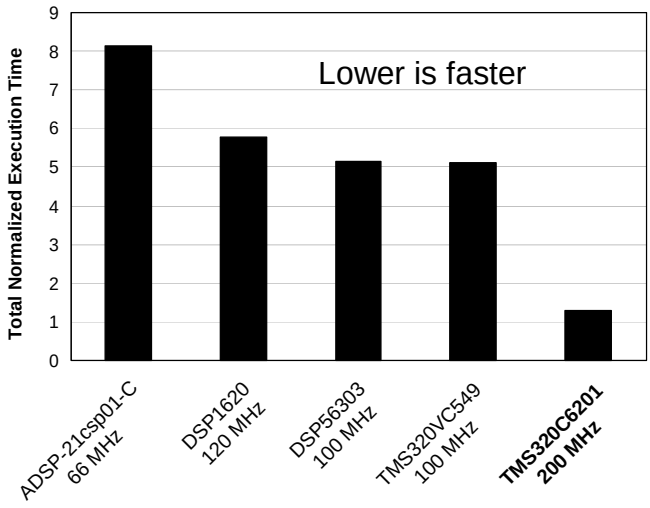
Total Normalized Execution Time



Analysis of Results

- The TMS320C62xx was the fastest DSP processor at the time it was introduced
- However, its speed was overstated
  - At 200 MHz, its speed would have been 4-6 times faster than the fastest DSPs available at that time
  - At 120 MHz, its speed was only 2-3 times faster than the fastest DSPs available at that time
- MIPS rating was highly misleading

Analog Devices ADSP-2116x

- Introduced in June 1998
  - Expected to sample at 100 MHz by 4Q98; first silicon delayed by about a year (and derated by 20 MHz)
- SIMD-enhanced version of ADSP-2106x (SHARC)
  - Duplicated data path of SHARC, widened buses

Twin data paths

  - Assembly-source-code compatible with SHARC
  - Reoptimization needed for SIMD
- First family member: ADSP-21160

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ADSP-2116x

"… as much as ten times higher performance than [the ADSP-2106x]"

– June 1998 ADI press release

"0.46 µs FFT"

(Benchmark result for 1024-point FFT, apparently based on 200 MHz clock)

– June 1998 ADI press release

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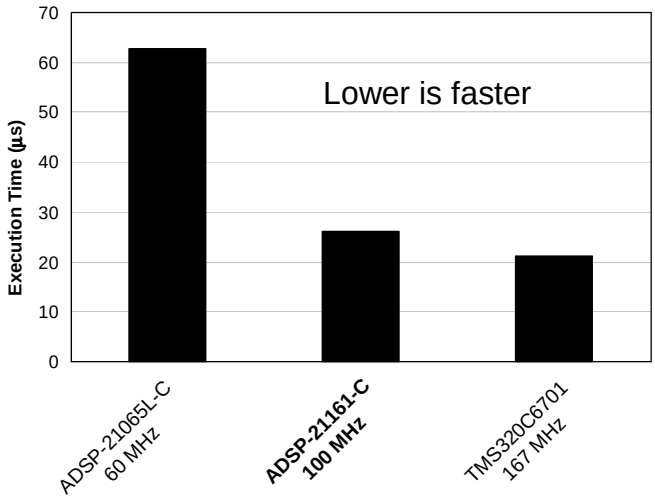
256-Point FFT Benchmark



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Analysis of Results

- To achieve 10x the performance of the ADSP-2106x in this benchmark, the ADSP-2116x would have to operate at roughly 400 MHz, four times the current clock speed

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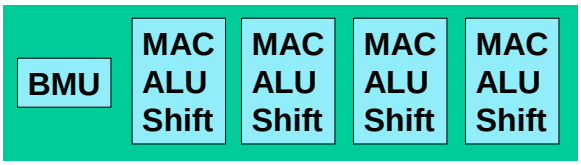
StarCore SC140 Core

- Up to 6 instructions per cycle
  - Fewer than the 'C62xx, but more powerful
  - 4 MACs/cycle vs. 2 for the 'C62xx
- Short (5-stage) pipeline



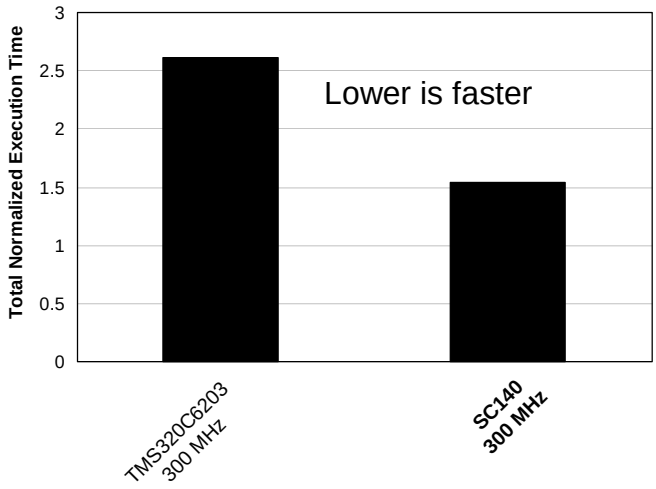
SC140

"The SC140 boasts the highest performance of any DSP core to date"

– April 1999 StarCore backgrounder describing the SC140 architecture

- Based on 300 MHz, 3000 "MIPS"

Total Normalized Execution Time



Analysis of Results

- At the time the SC140 was first fabricated, it was in fact the highest performance mainstream DSP core

Texas Instruments TMS320C64xx

- Upgrades the TMS320C62xx
- Announced in February 2000, with a projected speed of 1.1 GHz
- Still an 8-issue architecture, but each instruction and execution unit can do more
- New instructions support SIMD
  - Including four 16x16 or eight 8x8 multiplies per cycle
- Object-code compatible with 'C62xx
- Uses dynamic caches

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TMS320C64xx

"10 times the performance of today's fastest DSP"

– February 2000 TI press release

- Based on 1.1 GHz; initial chips sampling at 600 MHz

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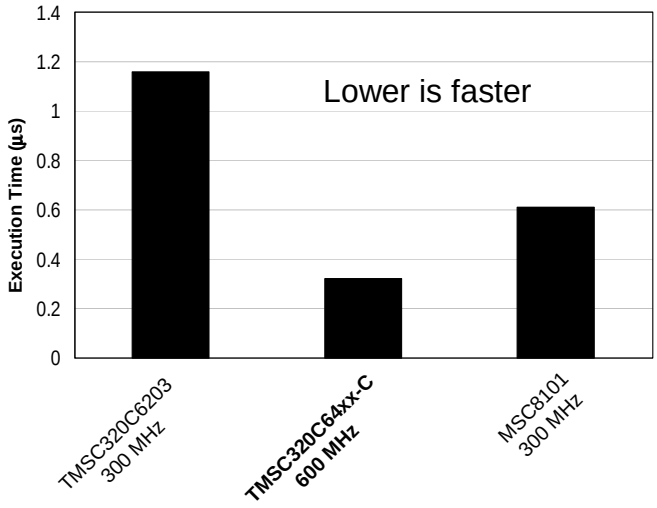
Real Block FIR Benchmark



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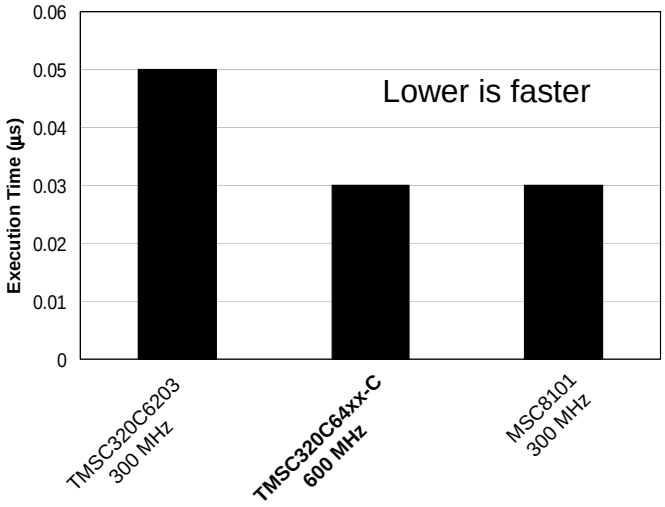
Two-Biquad IIR Benchmark



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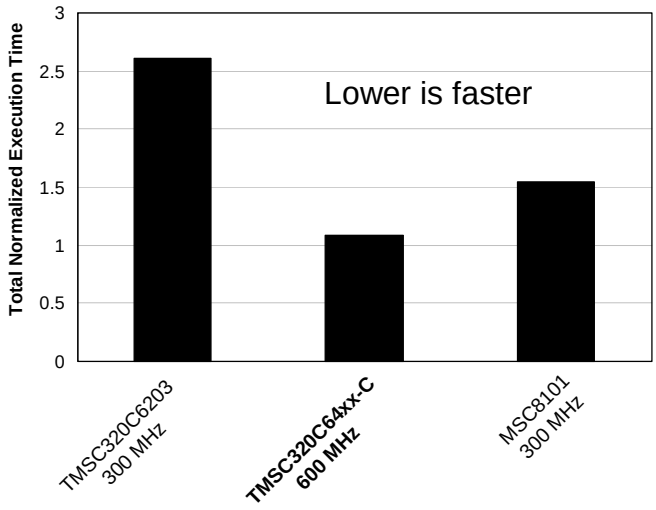
Total Normalized Execution Time

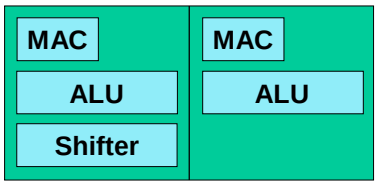


Analysis of Results

- At 600 MHz with L1 cache preloaded, the TMS320C64xx is about
  - 2.5 times faster than the TMS320C6203
  - 1.5 times faster than SC140
- To achieve ten times the speed of the TMS320C6203, the TMS320C64xx would have to operate at roughly 2.5 GHz and avoid L1 cache misses

Micro Signal Architecture

- Initial core (“Frio”) has two data paths
- 16-, 32-, and 64-bit mixed-width instruction set
- “Dynamic power management”
  - Initial chips operate between 300 MHz at 1.5 V and 100 MHz at 0.9 V
- MMU and mode-dependent instructions
- Memory configurable as SRAM or as cache



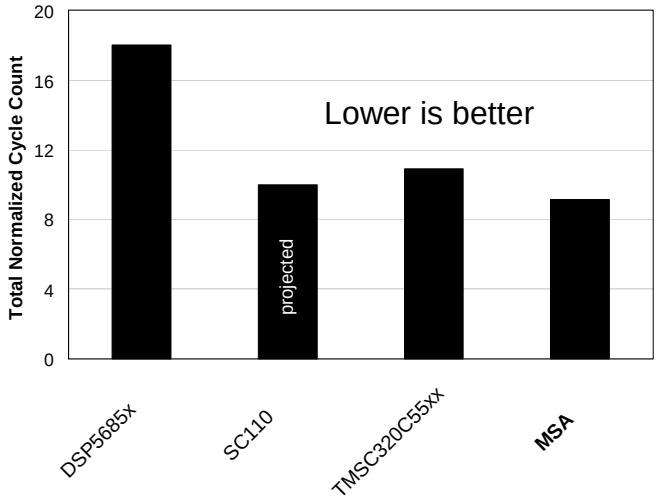
Micro Signal Architecture

“Per Cycle Benchmarks are unbeaten by competitors...

...20% to 80% fewer cycles required”

– December 2000 ADI/Intel MSA launch slides

Total Normalized Cycle Counts



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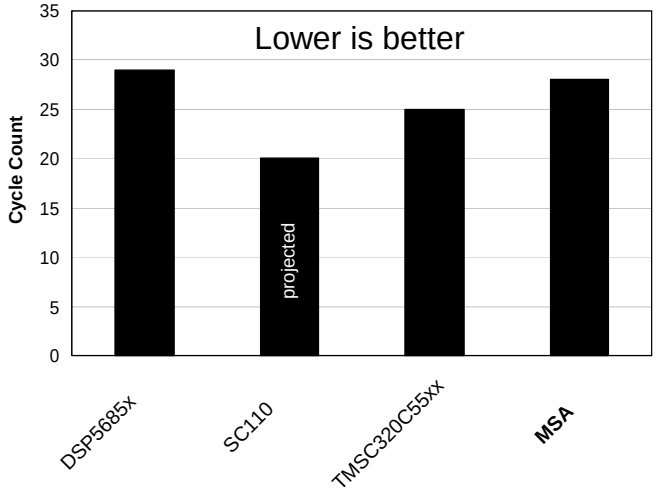
Single Sample FIR Benchmark



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Analysis of Results

- The MSA cycle counts are about
  - 50% lower than those of the DSP5685x
  - 10% lower than those of the SC110
  - 15% lower than those of the TMS320C55xx
- The MSA cycle counts are not consistently lower than those of the SC110 or the TMS320C55xx

Energy Consumption

- Power vs. energy
  - Energy considers both instantaneous power and the time required to complete a task

$$\text{Energy} = \int_0^T \text{Power}$$

- Vendors quote power, but we evaluate energy, since it is typically more useful

Texas Instruments TMS320C55xx

- Introduced in Feb 2000, with projected speed of 160-200 MHz—currently sampling at 200 MHz
- Based on TMS320C54xx, but with significant enhancements
  - Dual-issue VLIW
  - Dual MAC units
- Complex, compound instructions
  - Assembly source code compatible with 'C54xx
  - Mixed-width instructions: 8- to 48-bit

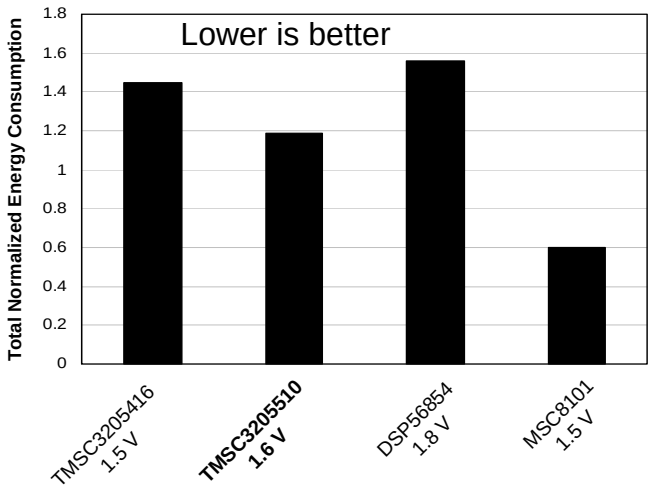
TMS320C55xx

"… requires only 15 percent of the power of the most power-efficient DSP available today"

– February 2000 TI press release

- Voltage not specified

Total Normalized Energy Consumption



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Analysis of Results

- Current 1.6-volt TMS320C55xx chips are not dramatically more energy efficient than TMS320C54xx chips
- Motorola's DSP56854 comes close to energy efficiency of TMS320C5510
- MSC8101 is much more energy efficient than the TMS320C55xx

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Memory Usage

- Why is memory use important?
  - Chip, system cost
  - Energy consumption
  - Speed
- Factors that affect memory use results
  - Instruction word width
  - Instruction-set style
  - Instruction-set efficiency for task at hand
  - Data word size
- ROM vs. RAM usage

Memory Usage Claims

- TMS320C55xx: “30% less compiled code size per function for control code (compared to the ‘C54xx)”

  – February 2000 TI slideshow describing the TMS320C55xx

- TMS320C64xx: “25% smaller code than [the TMS320C62xx]” (in compiled code; 15% from architectural improvements)

  – November 1999 TI slideshow describing the TMS320C64xx

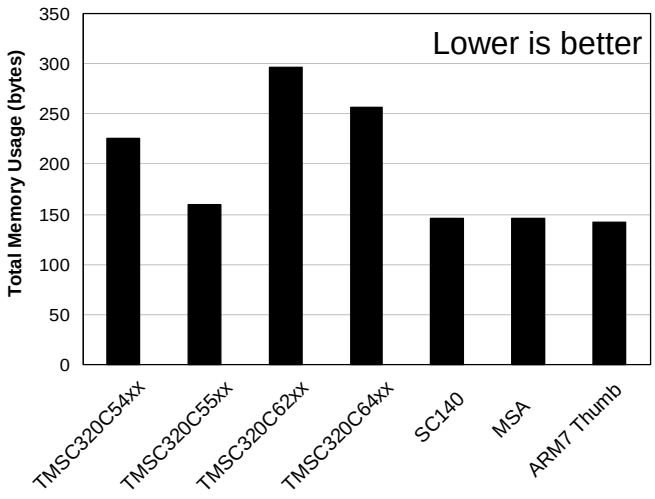
- SC140: “the SC140’s code is more than twice as dense as competing high-performance DSPs”

  – StarCore backgrounder describing the SC140 architecture

- MSA: “code density comparable to ARM7 Thumb”

  – December 2000 ADI/Intel MSA launch slideshow

Control Benchmark



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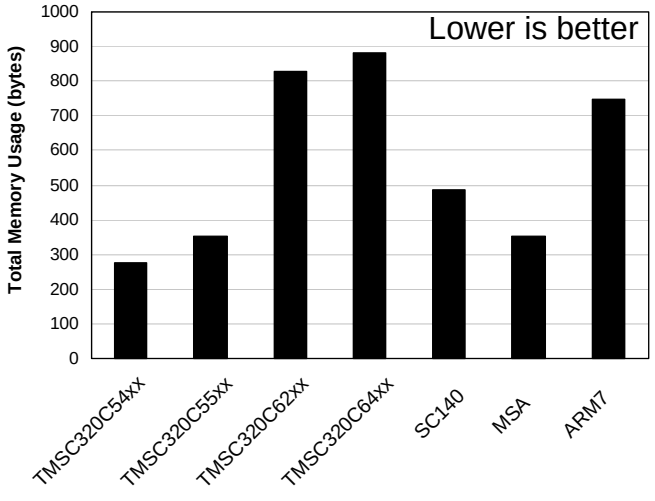
Real Block FIR Benchmark



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Analysis of Results

- Control Benchmark
  - 'C55xx uses 35% less memory than 'C54xx
  - 'C64xx uses 15% less memory than 'C62xx
  - SC140 uses about half as much memory as 'C64xx and 'C62xx
  - MSA memory use is similar to ARM7 Thumb
- Block FIR Filter benchmark
  - 'C64xx and 'C55xx both use more memory than predecessors; this will be typical in DSP algorithm code

Conclusions

- Be wary of vendor performance claims, particularly those related to speed and power consumption
- MIPS and MOPS are no longer meaningful
- Benchmarks are a key tool for assessing performance, but can be misused
- Comparing future processors with today's competitors is misleading
  - Competitor speeds may increase in the interim
  - Vendors may have difficulty producing full-speed silicon on time (or at all)

For More Information... www.BDTI.com

- White papers on DSP processor architectures and benchmarking
- Article reprints on DSP-oriented processors and apps
  - *Microprocessor Report*
  - *IEEE Spectrum*
  - *IEEE Computer* and others
- *comp.dsp* FAQ
- BDTImark2000™ scores